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DESIGN, DEVELOPMENT AND FABRICATION OF FAST SILICON POWER TRANSISTORS

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I. ABSTRACT

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This report summaries the development of the 20-ampere silicon switching transistor by RCA, Electronic Components and Devices, Somerville, New Jersey. The first section of the report describes the theory that resulted in the final design of the device. The next two sections describe the device fabrication procedures, including a description of the experimental work that led to the final processing techniques. The last section presents the testing methods used and an evaluation of the 45 prototype samples delivered to the contracting agency.

Author

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II. PURPOSE OF THE CONTRACT AND MAJOR TECHNICAL OBSTACLES ENCOUNTERED

A. PURPOSE

The purpose of this contract is to design, develop and fabricate a fast switching (20-ampere) transistor, preferably mounted in an isolated collector package capable of high power dissipation. Because of its potential military and space applications, high reliability and reproducibility of the device are to be prime considerations of the program.

The program required delivery of five prototype samples and forty-five production units which conform to the following requirements:

1) General Requirements: Physical size to be as small as possible to meet electrical and mechanical requirements.

2) Mechanical Specifications:

	Initial	Final
a) Sealing	Hermetic	Hermetic
b) Material	Silicon	Silicon
c) Terminals	Jedec-flag type	Spade type
d) Case	Stud mounted DES	Stud mounted DES

3) Electrical Specifications:

a) $V_{CE(SAT)}$ at I_C = 20 amperes, h_{FE} = 10 (min.)	1.5 volts (max.)	1.5 Volts (max.)
b) Collector to Emitter Voltage (V_{CES})	200 volts	125 volts
c) Collector Current (I_{CBX})	30 ma (max.)	30 ma (max.)

	at V_{CE}	200 volts	125 volts
	T_j	150°C	200°C
	V_{EB}	-1.5 volts	-1.5 volts
d)	Emitter Current (I_{EBO})	25 ma (max.)	25 ma (max.)
	at V_{EB}	10 to 15 volts	10 volts
	T_j	150°C	200°C
e)	Base Voltage (V_{BE}SAT)	3.5 volts (max.)	3.5 volts (max.)
f)	Turn on Time ($t_d + t_r$)	0.25 μsec. (max.)	0.25 μsec. (max.)
	I_C = 20 amps, I_B = 2 amps,		
	V_{CE} = 120 volts		
g)	Turn off time ($t_s + t_f$)	0.25 μsec. (max.)	0.25 μsec. (max.)

4) Thermal Characteristics

a)	Grounded Collector	
	Power dissipation (P_c)	250 watts	250 watts
	Thermal Resistance (θ_{J-C}) Maximum	0.45°C/W	0.66°C/W
	Thermal Resistance (θ_{J-C}) Typical)	0.22°C/W	— —
	Thermal Capacitance (C_t)	0.6 watt-sec/°C	0.6 watt/sec/°C
	Thermal Time Constant (T_{J-C})	120 msec.	120 msec.
b)	Isolated Collector		
	Power Dissipation		145 watts
	Thermal Resistance		1.2°C/W

5) Environmental Specifications

a)	Temperature Cycling (5 cycles)	-65 to + 150°C	-65 to + 200°C
b)	Moisture Resistance (10 cycles)	— —	— —
c)	Centrifuge (10,000 g)	— —	— —
d)	Storage Life (1000 hours)	+ 150°C	+ 200°C
e)	Shock (500 g)	— —	— —
f)	Vibration (2o g, 100 to 2000 cps)	— —	— —

B. MAJOR TECHNICAL OBSTACLES ENCOUNTERED

RCA's long and varied experience in the development, refinement and production of silicon power transistors has led to a firm conviction that planar passivated structures will result in devices with the greatest reliability. Furthermore, the control of tolerances obtainable with the planar fabrication technique, yields devices which combine excellent characteristics with tight parameter distributions. Although the desired device parameters could be attained by employing conventional mesa techniques, a planar transistor appeared to be more advantageous for fulfilling the contract objectives.

There were two major limitations in the fabrication of large area planar transistors: 1) low yields in the diffusion processing and 2) low breakdown voltage. The problem of low breakdown voltage was of no great concern on this device because the specified 125-volt requirement is within the recognized planar limitation of 150 to 200 volts. Therefore, the most

severe obstacle encountered in the fabrication of this device, utilizing planar technology, was the need to solve the widely reported diffusion yield problem. The literature on this subject indicates that devices with collector areas of approximately 10,000 square mils are impossible to make, with reasonable yields. During this contract program, techniques and skills were developed which made it possible to fabricate the desired large area devices as a planar transistor, with good yields.

Another problem area was anticipated in the packaging of the unit. The specific problem involved the request that the unit be encased in an isolated collector package with low thermal resistance. This required the development of a new packaging technology. The proper materials had to be selected, the problem of thermal mismatch had to be solved and the mechanical strength had to be resolved before this package would become a reality.

III. DESIGN CONSIDERATIONS

A. DEVICE DESIGN

The design of a transistor is a compromise between the dictates of device theory and the limitations of processing technology. Because of a continued need for better, more reliable transistors, processing technology has undergone rapid advancements in recent years. The development of the triple-diffused or double-diffused epitaxial type transistor ,combined with planar oxide passivated techniques,has radically tightened practical geometric tolerances. The utilization of photolithographic systems for dimensional control has afforded the ultimate in processing capability.

The following section describes the theory that lead to the design of the 20-ampere switch. Reference will be made to the practical aspects of device technology, indicating where safety factors and empirical data have dictated the final design. Processing relationships will be interrelated with transistor device theory to give a complete picture of how the TA 2438 transistor has evolved. A comparison of computed to actual electrical characteristics is presented in an effort to show both the success of the transistor and the areas where more work is required.

1. Thermal Resistance

The first consideration in designing a transistor pellet is to determine the pellet area necessary to dissipate the required power. The final

thermal resistance requirement stipulated for the 20-ampere switch is 1.2°C/watt in an isolated collector package. The initial stud was a large, rather heavy 1-1/16 DES type. This was changed to a smaller, lighter 11/16" DES type which required a higher thermal resistance limit. A calculation of the minimum required area is shown below for a pellet mounted in a copper 11/16" DES case, with beryllium oxide collector insulation. The following approximations have been made:

1) Heat flow does not diverge in the silicon or beryllia (planar heat flow).
2) The average heat flow path through the DES case diverges at an angle such that the effective copper heat transfer area is twice the area of the silicon pellet.
3) All interfaces conduct perfectly.
4) Conductivities are not impaired by alloy formation at the interfaces.

Thermal resistance in a one-dimensional system can be calculated from the following equation.

$$\theta = \frac{T}{Q} = \frac{1}{K}\frac{X}{A} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (1)$$

where θ is the thermal resistance in °C/watt,

K is the thermal conductivity in watts-cm/°C,

X is the thickness of the material in centimeters,

A is the cross sectional area in centimeters squared,

T is the temperature rise, and

Q is the power flow rate.

The thickness and thermal conductivity values of silicon, beryllia and copper are indicated in Table I.

TABLE I

MATERIAL THICKNESS AND THERMAL CONDUCTIVITY

Material	X (Thickness in cm)	K(Thermal Conductivity in Watts/cm°C
Silicon	15×10^{-3}	0.84
Beryllia	127×10^{-3}	2.10
Copper	450×10^{-3}	3.80

If we assume A_{eff} Cu = $2A_{si}$ and A_{eff} BeO = A_{si}, then we can calculate the required pellet area from

$$\theta_{overall} = \left[\frac{X_{si}}{K_{si} A_{si}} + \frac{X_{BeO}}{K_{BeO} A_{si}} + \frac{X_{cu}}{K_{cu} 2A_{si}} \right] \quad \ldots\ldots\ldots (2)$$

as follows:

$$A_{si} = \frac{1}{\theta} \left[\frac{X_{si}}{K_{si}} + \frac{X_{BeO}}{K_{BeO}} + \frac{X_{cu}}{2K_{cu}} \right]$$

$$A = \frac{1}{1.2°C/W} \left[\frac{15 \times 10^{-3}}{0.84} + \frac{127 \times 10^{-3}}{2.1} + \frac{450 \times 10^{-3}}{2 \times 3.8} \right]$$

$$A = 0.112 \text{ cm}^2$$

The reliability of the assumptions determine how closely the calculated value will approach the actual result. The divergence of the heat flow through the copper (accounted for by the factor of 2 in the area) is an approximation because the true thermal paths through the stud are difficult to calculate.

Observed variations in thermal resistance can generally be attributed to invalidity of approximations 3 and 4. Due to incomplete wetting and voids in the alloyed joints the heat transfer area can be considerably reduced. The alloys also have a significant thickness and their thermal conductivities can be considerably decreased due to micro-grain structures.

Several device structures were designed, using the calculated base area of 0.112 cm^2 as a basis. The final device, the TA 2438, has a base area of 0.120 cm^2.

The actual values obtained from thermal resistance measurements made on final units showed excellent agreement with the calculated result. The median thermal resistance was 1.18°C/W (see Figure 1). The distribution was quite tight, with 90% of the units falling within the range 1.2 ± .4°C/W. The few units that were above this value resulted from incomplete alloy interfaces due to uneven wetting. Because the area of the beryllium oxide pellet was actually larger than the pellet itself, some of the units were below the calculation value of 1.2°C/W. The assumption that thermal spreading effectively doubles the copper induction path area is a conservative estimate.

2. Collector Breakdown

The maximum voltage which a transistor will withstand is the breakdown voltage of the collector junction. This voltage is governed by the resistivity on either side of the junction, the doping gradient on both sides of the junction and surface effects. The NP$\bigcup$N diffused

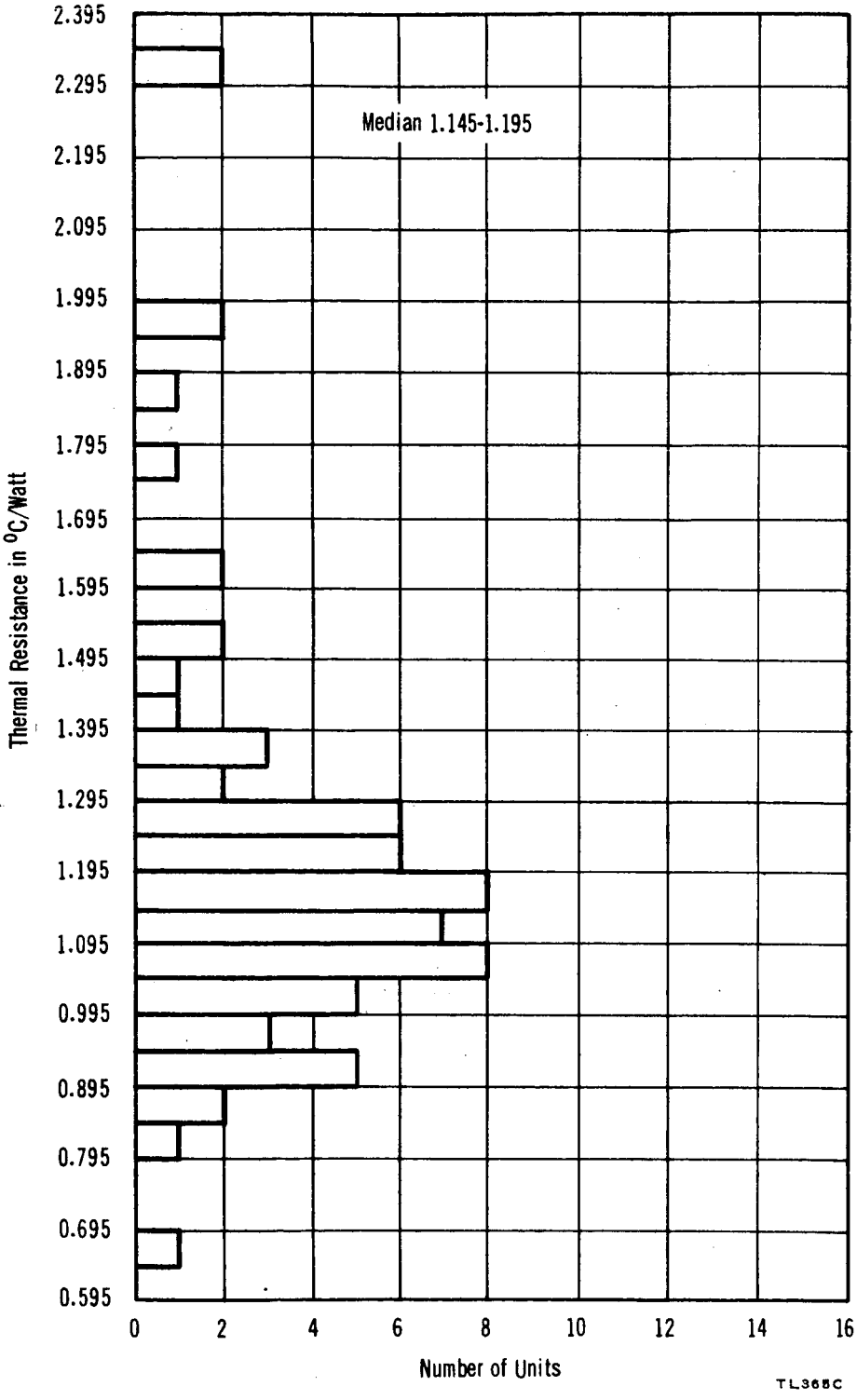


FIGURE 1 THERMAL RESISTANCE HISTOGRAM

structure used in this device has a narrow, heavily doped diffused base region to optimize the high-current switching characteristics. The base is much more heavily doped than the collector ν region, therefore, the depletion layer spreads mostly into the lightly doped collector region.

The diffused base layer in this device goes approximately 0.2 mils deep with a surface concentration of about 7×10^{17} atoms/cm^3. The calculation of avalanche breakdown voltage can be made, using the relationship between these two parameters and the background resistivity as shown by Kennedy and O'Brien[1].

It is interesting to note, however, that if breakdown voltage is calculated, assuming an abrupt p+n junction, i.e. no diffusion gradient, a value which is almost identical to that using the Kennedy and O'Brien curves is obtained.

ABRUPT JUNCTION	DIFFUSED JUNCTION (Kennedy and O'Brien)
ρ collector = 3.5 ± .5Ω-cm, N Type	C surface of base = 7×10^{17}/cm^3
C collector = 1.5×10^{15} atoms/cc	C collector = 1.5×10^{15}/cm^3
BV_{CBO} = 260 volts	X_j = junction depth = 0.2 mils
W(depletion layer width) = 0.58 mils	BV_{CBO} = 270 volts
	W(depletion layer width) = 0.5 mils

These values are so close that the avalanche breakdown voltage is dependent almost exclusively on the resistivity of the n-side of the junction. The spread of the depletion layer into the base and the collector can be determined by using the relationships and curves of Lawrence and Warner[2] and the resisitivity values shown above. A Gaussion base diffusion, resulting from a finite surface concentration, and a voltage of 250 volts is assumed. Table II summarizes and compares the results of these three calculations.

TABLE II

COMPUTED VALUES OF BV_{CBO} AND DEPLETION LAYER SPREAD

Reference	Collector Resistivity (ohm-cm)	Base Surface Concentration (/cm^3)	BV_{CBO} (volts)	Depletion Layer Width (in mils)		
				p side	n side	total
Kennedy and O'Brien	3.5	7×10^{17}	270	—	—	0.5
Abrupt Junction	3.5	—	260	—	0.58	0.58
Lawrence and Warner (Gaussion Distribution)	3.5	7×10^{17}	assumed 250	0.09	0.54	0.63

In order to achieve maximum junction breakdown, the spread of the depletion layer should not be restricted by its extension into silicon, which has decreasing resistivity. The calculated values of depletion layer spread are in close agreement and show that the space charge layer is 0.5 to 0.6 mil wide at breakdown. This value dictates that the minimum thickness of the high resistivity region of the collector body must be 0.6 mil if true avalanche breakdown is to be reached.

In practice, however, planar, oxide-passivated junctions do not reach 250-volt breakdown when 3 to 4 ohm-centimeter material is used. Planar devices made with 3 to 4 ohm-centimeter material show a fairly tight BV_{CBO} distribution of approximately 100 to 125 volts. The difference between the theoretical value of 260 volts and the actual value of 120 volts is due to inversion and/or enhancement layers established during oxide growth, to surface imperfections, and to surface field effects arising from device processing. Junction breakdown occurs when the maximum field is reached at the surface, and this occurs at a lower applied voltage than

dictated by bulk considerations.

Assuming an average actual breakdown of 110 volts, depletion layer spreads have been calculated for 3.5 ohm-centimeters as follows:

	Diffused	Abrupt
Total Depletion Layer Width	0.43 mils	0.38 mils
Base " " "	0.07 mils	
Collector " " "	0.36 mils	0.38 mils

The thickness of the collector region has been designed to be greater than 0.4 mil in the TA 2438.

3. Collector Capacitance

The expression for the capacitance of a p-n junction is identical to that for a parallel plate capacitor, with the depletion layer width analogous to the distance between the plates. This expression is

$$C = \frac{\epsilon \epsilon_o}{W} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (3)$$

where W is the total depletion layer width,

ϵ_o is 8.85×10^{-14}, and farads/cm and

ϵ is the dielectric constant of silicon (12).

However, the distance between plates, i.e. depletion layer width, in a p-n junction is voltage dependent, therefore the capacitance is voltage dependent.

A plot of capacitance versus voltage from 1 to 100 volts was constructed from data taken on TA 2438 transistors and compared to the values obtained from the graphs of Lawrence and Warner, assuming a Gaussian distribution. A logarithmic plot (see Figure 2) shows parallel lines with a relationship of $C\alpha V^{-0.41}$ for both the calculated and measured junctions. This means that the change in the TA 2438 junction depletion layer spread with voltage, which had been previously assumed, obeys the relationship of a Gaussian type base diffusion.

The calculated collector capacitance is in good agreement with the measured capacitance.

A comparison of the theoretical C versus V relationships for abrupt junction and linearly graded junctions to those obtained from the measurements is as follows:

Abrupt $C = V^{-0.5}$

TA2438 $C = V^{-0.41}$

Linear $C = V^{-0.33}$

This comparison agrees with the calculations of collector breakdown voltage in that the p-type gradient at the junction is quite steep. It approaches an abrupt type junction.

4. Emitter-Base Breakdown Voltage

The emitter base breakdown voltage in a switching transistor limits the maximum turn-off voltage that can be used. The contract require-

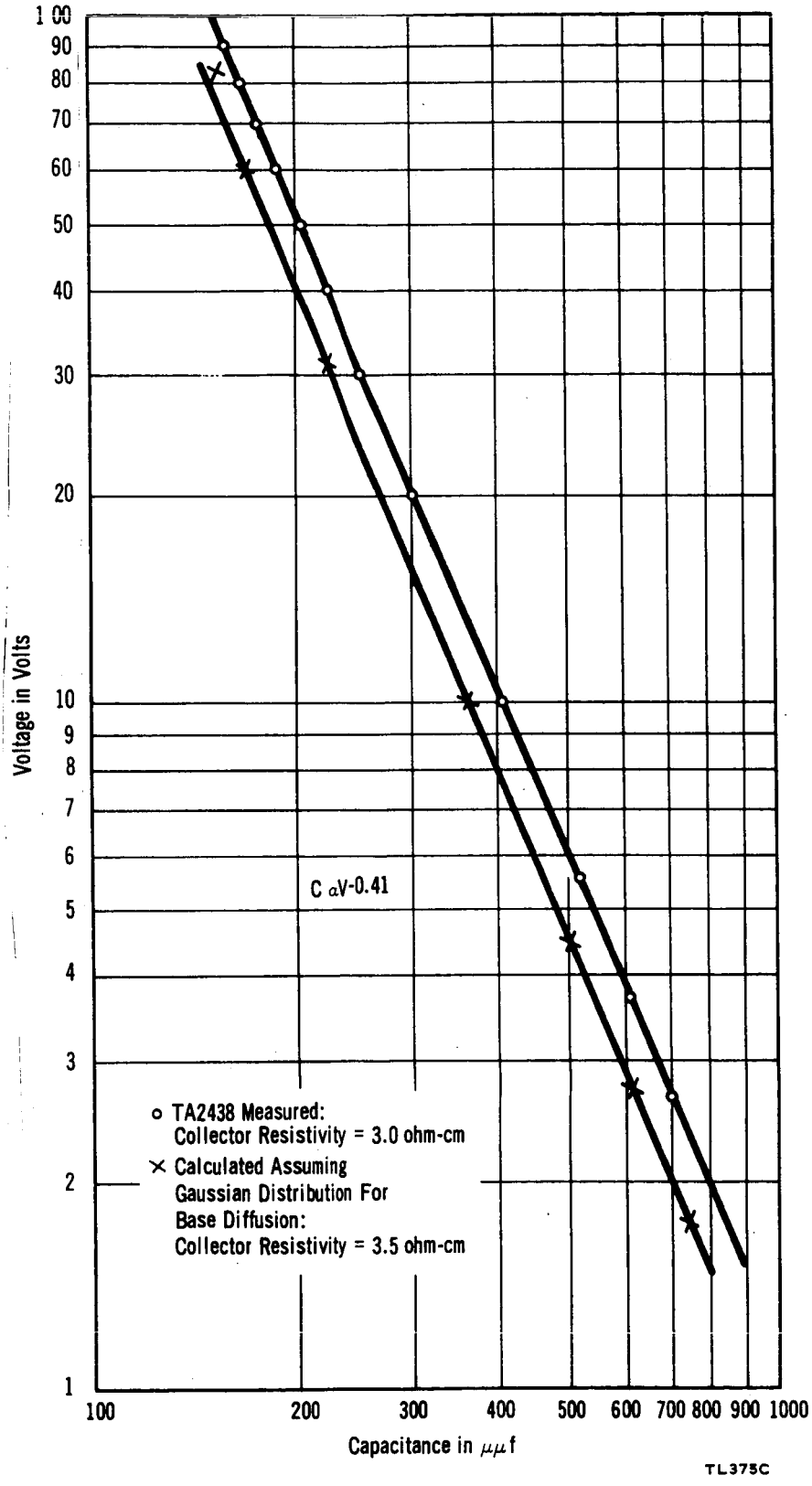


FIGURE 2 COMPARISON OF THEORETICAL VS. ACTUAL COLLECTOR CAPACITANCE AND VOLTAGE OF A TA2438 UNIT

ment for this transistor was 10 volts at 200°C. The emitter-base breakdown is determined by resistivities on both sides of the junction and gradients at the junction.

In the fabrication of a transistor, the emitter concentration is generally kept as high as possible and the base is kept as low possible in order to attain a high injection efficiency. The concentration of impurities on both sides of the junction is dependent on impurity diffusion profiles. It has already been shown that the base surface concentration is 7×10^{17} atoms/cm^3. The breakdown will be determined mostly by the highest concentration on the base side of the junction. Due to the diffusion gradient on the base, this occurs at the surface where the base concentration is highest. The emitter is diffused with the maximum surface concentration maintained throughout the diffusion. The emitter penetration is one-half the base depth and the final surface concentration of the n-type diffusant is 2×10^{21} atoms/cm^3. Utilizing these values, the nomograph of Kennedy and O'Brien[1] can be applied to determine the value of breakdown voltage. In such a calculation:

C_S emitter = 2 x 21 atoms/cc

C_S base = 7×10^{17} atoms/cc

X_J = Junction depth 0.09 mils

BV_{EBO} = 12.5 volts

The actual value obtained from the finished units was in the vicinity of 10 volts at true breakdown. Some units had surface defects which

led to high leakage currents, and lower apparent breakdown.

5. Current Gain

The switching time calculations of storage time (see Section III-10) indicate that the current gain should be as low as possible at the 20-ampere level. However, the saturation voltage requires the current gain to be a minimum of approximately 18.

The first-order expression for the current gain of an npn transistor which neglects the effect of current crowding is given by Webster[3] as

$$\frac{1}{\alpha_{CB}} = \frac{SAsW}{D_n A} + \frac{\sigma_b W}{\sigma_e L_e} + \frac{1}{2}\left(\frac{W}{L_b}\right)^2 \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (4)$$

$$\alpha_{CB} = \delta I_C / \delta I_B$$

where S is the surface recombination velocity,

A is the area in square centimeters

A_s is the area of surface recombination,

D_n is the diffusion constant of electrons in the base,

σ_b is the conductivity of the base,

σ_e is the conductivity of the emitter,

W is the base width,

L_e is the diffusion length of holes in the emitter, and

L_b is the diffusion length of electrons in the base.

The first term relates the effect of surface recombination on gain and is very important at low currents. At higher currents the surface effect is reduced and the other two terms dominate. The second term describes the effects of emitter efficiency and the third term describes the effects of recombination in the base region. Because of the extremely long emitter edge in this device, the effective area for surface recombination, A_s, is quite large. This results in a surface dependent current gain at collector currents up to one ampere.

The second term relates current gain to the emitter efficiency. From this expression it can be seen that at high currents, the base conductivity (σ_b) will be modulated, thereby lowering the gain. The third term relates the base transport factor to current gains. In this expression we see a relationship of lifetime and basewidth, both of which are relatively independent of the current level.

The maximum gain will occur at a current level, after surface recombination no longer dominates and before conductivity modulation decreases the current gain. Because the emitter is heavily doped, it is expected that the maximum current gain will be dependent, primarily, on the base transport factor. Thus

$$\frac{1}{\alpha} = \frac{1}{2}\frac{W^2}{L} = \frac{W^2}{2 D_n \tau_b} \qquad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (5)$$

If

$$D_{n\,b} = 15 \text{ cm}^2/\text{sec.}$$

$$\tau_b = .2 \times 10^{-6} \text{sec.}$$

$$W = 2.5 \times 10^{-4} \text{ c,}$$

then

$$\frac{1}{\alpha_{CB}} = \frac{1}{2} \frac{(2.5 \times 10^{-4})^2}{15 \times .2 \times 10^{-6}}, \quad \alpha_{CB} = 100$$

Two interesting comparisons can be made between calculated and actual gain dependencies. Figure 3 plots 1 and 20-ampere current gains (which are usually equal) and 5-ampere current gains. The 45° slope reflects the equality of the 1, 5 and 20-ampere gains. However, in the range 0.01 to 1 ampere, current gain rises as a function of current due to the surface effects. At high currents the base transport factor limits the gain (see Figure 4). The fact that there is very little change in gain with increasing current at high injection levels, agrees with the assumption that the emitter efficiency term does not have a significant effect on the gain.

The deviation of the actual values of current gain to the calculated value is related to two factors. One is that the value for minority carrier lifetime is assumed and may not be an accurate number. The other factor is that the base width on many of the delivered units is wider than originally planned. This was done in order to reduce the gain and storage time. If a base width of 0.13 mil is used in the calculation, then $\alpha_{CB} = 58$. This is in closer agreement with the final data.

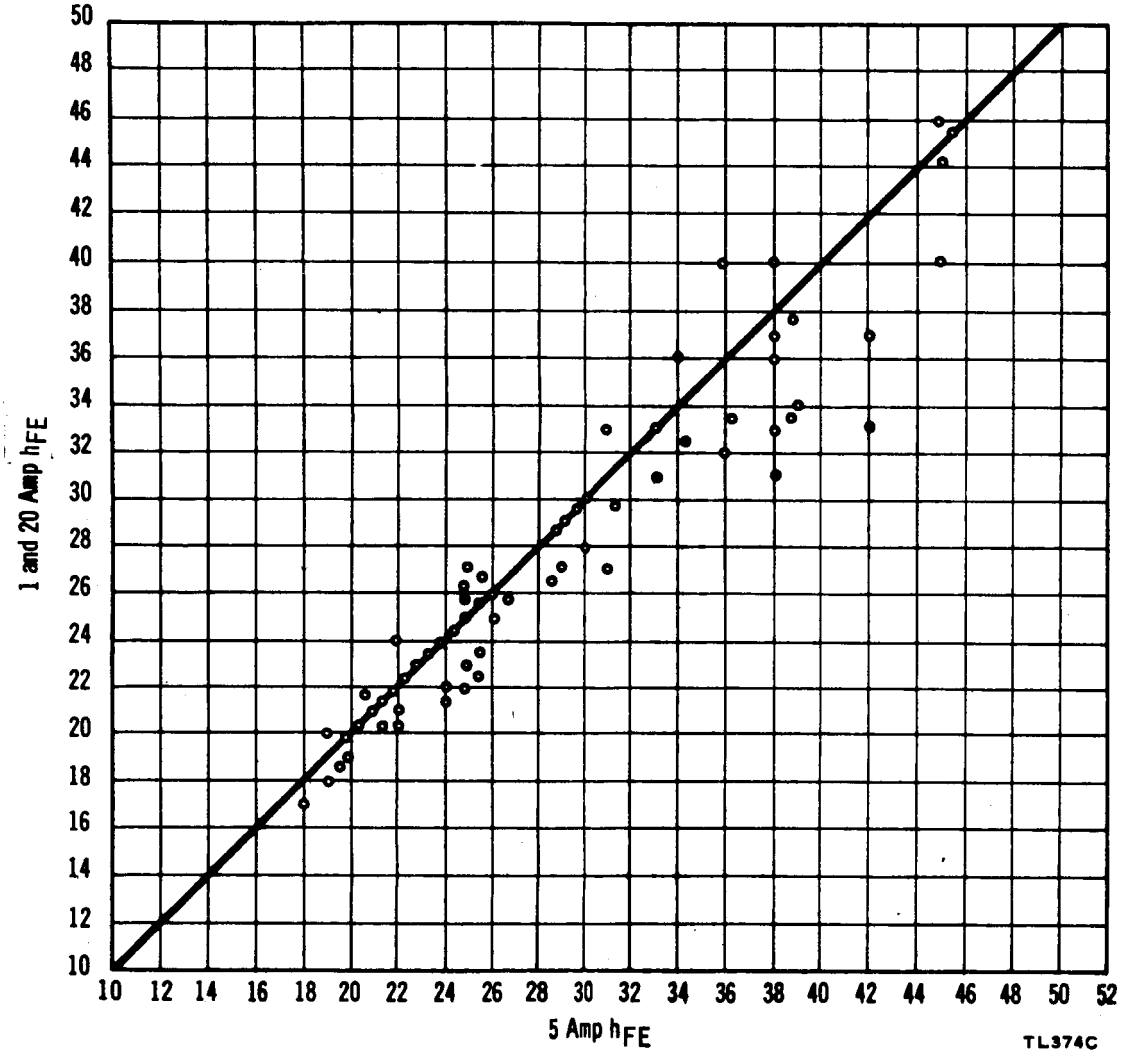


FIGURE 3 5 AMPERE CURRENT GAIN VS. 1 AND 20 AMPERE CURRENT GAIN

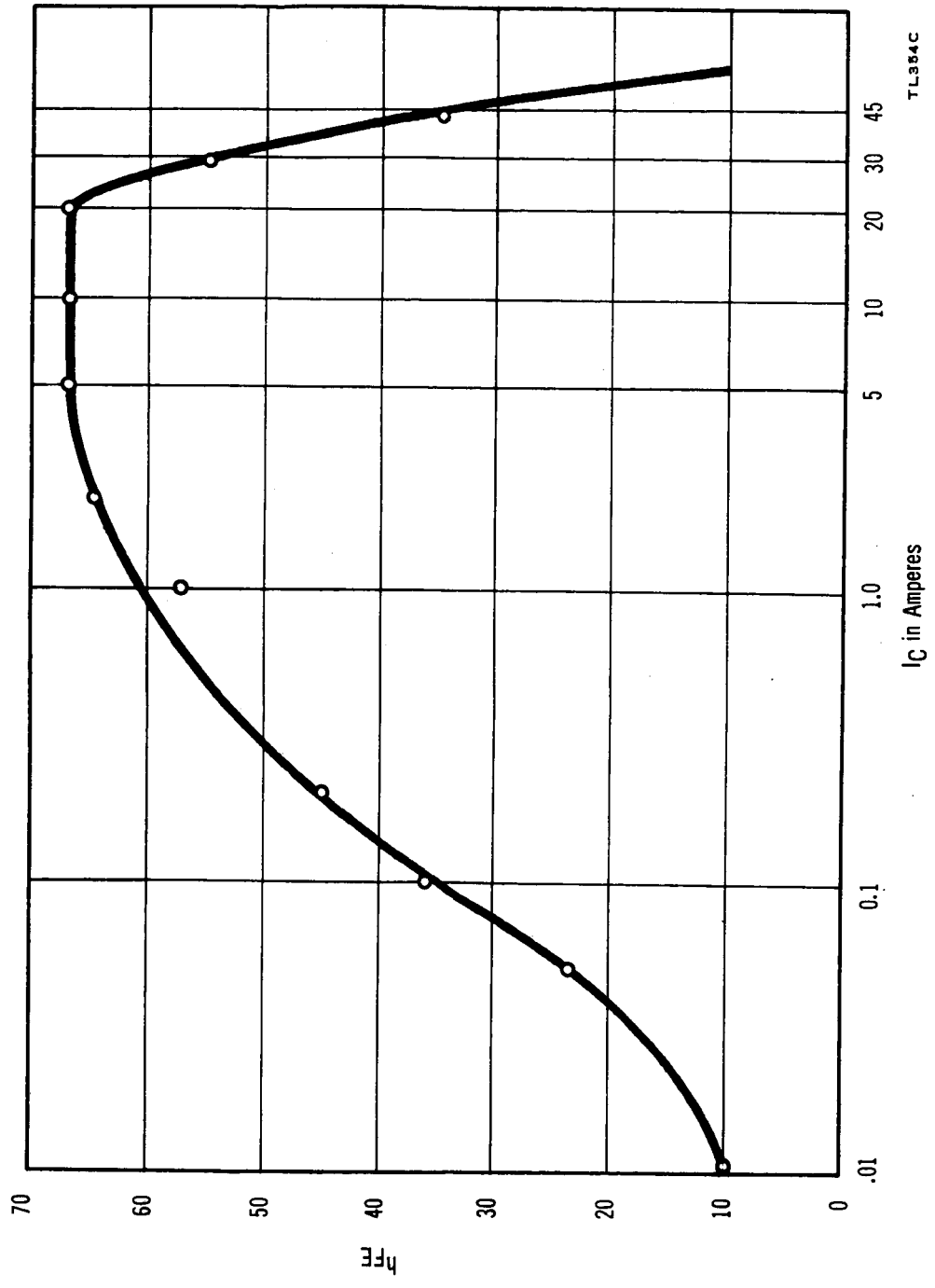


FIGURE 4 CURRENT GAIN VERSUS COLLECTOR CURRENT .01 AMP - 30 AMP.

6. V_{CEO} Sustaining

The sustaining voltage is another limiting factor of transistor operation. It is the steady state voltage across a transistor after the collector base junction has started to conduct. V_{CEO} is lower at high current then at low current, indicating that the transistor goes through a negative resistance region prior to achieving a steady V_{CEO} level.

The sustaining voltage is governed by two independent variables, the collector breakdown voltage and the current gain. The relationship, however, contains an empirical constant (n) which is related to the multiplication factor of the semiconductor material. Thus

$$V_{CEO} = \frac{BV_{CBO}}{(1 + h_{FE})^{1/n}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (6)$$

In order to calculate a V_{CEO} value, the correct variables must be chosen. Two questions arise in the selection of variables: 1) the current level at which the h_{FE} value should be taken and 2) the value of BV_{CBO} which should be inserted. It appears that the surface breakdown value is the correct one because the sustaining voltage relates to the field across the space charge layer of the collector, which is limited by the surface breakdown. The h_{FE} value of the transistor is current dependent, and at currents between 100 micro-amperes and 1 ampere the device does not have a specific h_{FE} value. Furthermore, the constant n is an empirical value and may vary for

different devices[4]. The value of n has been calculated for a transistor at 4 current levels. From the slope of the logarithmic plot of $(1 + h_{FE})$ versus $\frac{V_{CB}}{V_{CE}}$ illustrated in Figure 5, the value of n is shown to vary with current. The value, obtained at higher currents, is in agreement with the reported values of 4. Consequently, the data attributes part of the negative resistance region of the V_{CEO} characteristic to the change in the low level gain point as a function of current.

7. Collector to Base Reverse Current, I_{CBO}

The reverse-bias current of the collector-base junction of a transistor is frequently an indication of device stability and reliability. An ideal silicon junction will have extremely low reverse-bias currents at any voltage up to the breakdown region. The ideal saturation voltage is inversely proportional to the minority carrier lifetime on the lightly-doped side of the junction and directly proportional to the depletion layer width[5]. In the case of a p+n junction, the saturation current is dependent on the concentration of the n side.

The calculation of collector current is made at -50 volts, utilizing

$$I_{CBO} = q\ U\ W\ A \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (7)$$

where I_{CBO} is the reverse-bias collector-base current,

$q = 1.6 \times 10^{-19}$ coulombs,

W is the depletion layer width = 7.0×10^{-4} cm at 50V,

A is the collector-base area = .120 cm^2, and

$$U = \frac{P_i}{2(\tau_p)_n} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (8)$$

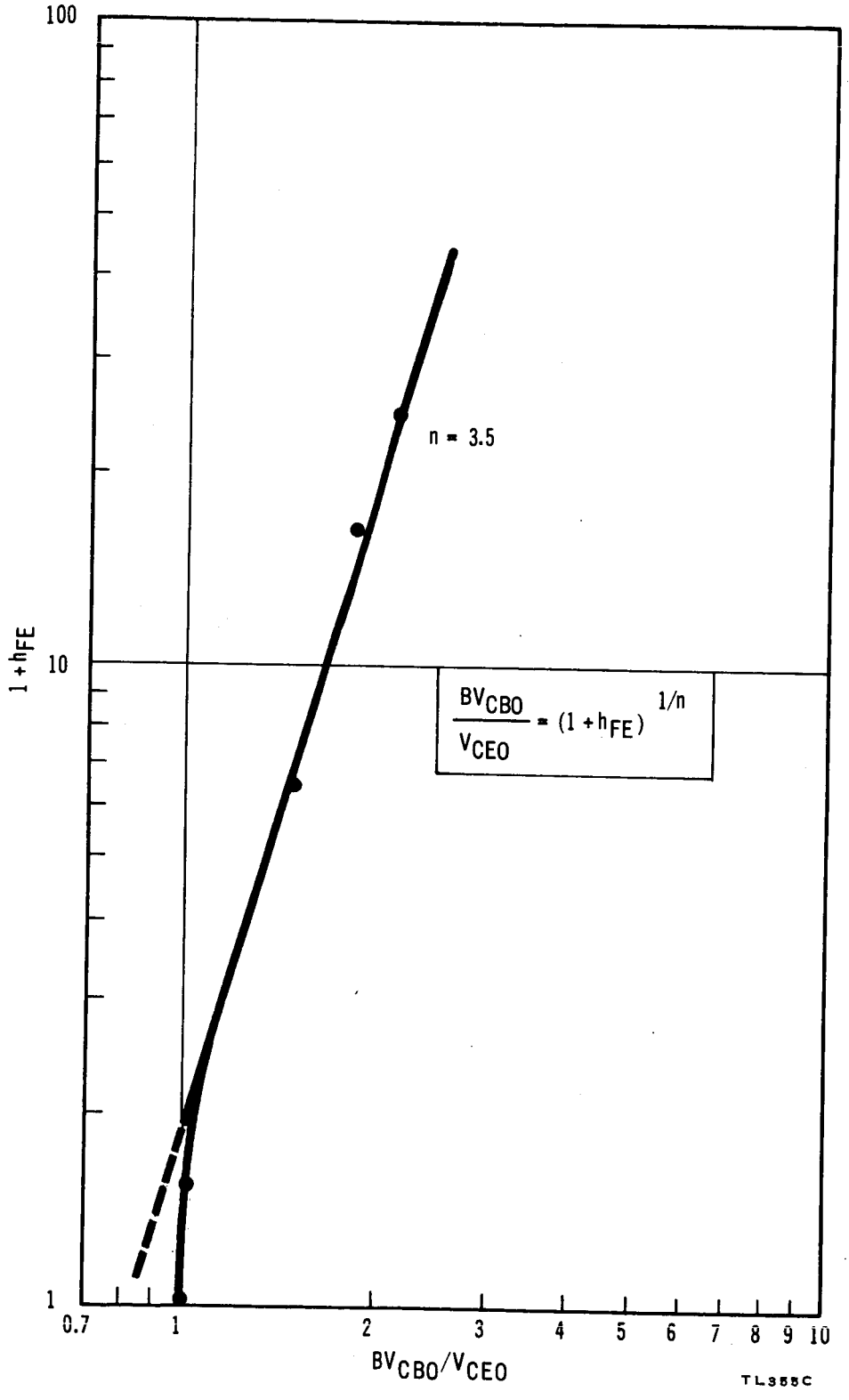


FIGURE 5 EVALUATION OF n FOR THE TA2438

where p_i is the intrinsic hole concentration = 1.4×10^{10} holes/cm^3, and τ_{pn} is the lifetime of holes on the n-side of the junction = 2×10^{-6} sec. Solving for I_{CBO}

$$I_{CBO} = 1.6 \times 10^{-19} \times \frac{1.4 \times 10^{10}}{2 \times 2 \times 10^{-6}} \times 7 \times 10^{-4} \times 1.20 \times 10^{-1}$$

$$I_{CBO} = 4.8 \times 10^{-8} \text{ amps.}$$

The median value of reverse-bias current on the final units is 2.5×10^{-8} amperes at -50 volts. This is an excellent example of the low stable leakage currents obtainable with planer, oxide protected surfaces. Surface leakage currents which result in much higher values have been a problem in mesa etched structures. This problem has been eliminated by planer units, when surface inversion layers are not encountered (Section VA4).

8. Saturation Voltage

The saturation voltage requirement for this transistor is less than 1.5 volts at 20 amperes with a base drive of 2 amperes. Decreasing the voltage drop across the transistor is a great advantage to circuit engineers because of the resulting increase in circuit efficiency.

The voltage drops in terminals, bonding wires and contact resistance makes up an appreciable amount of the voltage when 20 amperes is being conducted. The major design parameter to consider in limiting this value is the collector resistance. If a value of 0.8 mil thickness for the undiffused collector and a resistivity of 3.5 ohm-centimeters is assumed, the series resistance of the collector can be calculated as

$$R = \frac{\rho l}{A} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (9)$$

where R is the collector resistance,

ρ is the collector resistivity,

l is the collector thickness, and

A is the collector area

and solving for R

$$R = \frac{3.5\Omega\text{-cm} \times 2.0 \times 10^{-3}}{.113\ \text{cm}^2}$$

$$R = 0.062\ \Omega\ .$$

The required saturation resistance is less than 0.075 ohms (i.e. 1.5 volts at 20 amperes) which means that the collector series resistance is appreciable in the case where there is no conductivity modulation.

9. Design of Emitter Electrode

The concept of edge injection from the emitter at high current levels is the guiding design criterion for the geometry best suited to carry high currents. Fletcher has shown that voltages caused by lateral current flowing in the base results in the injection of current at the edge of the emitter[6]. This means that a device can carry a current which is proportional to the length of the emitter edge, rather than the area of the emitter.

The interdigitated structure has been developed for the purpose of producing a large emitter edge to emitter area ratio. Such a ratio permits high emitter injection with small device areas, thereby increasing frequency response, lowering storage time and sometimes reducing device costs. Previous experience with the interdigitated

geometry has resulted in an empirical relationship of emitter current to emitter periphery. From this data, the emitter was designed with a 2.5 to 3.0 inch periphery in order to satisfy the maximum current rating of 20 amperes. The tight dimensional tolerances obtained with standard photoresist techniques in the production of the comb type emitter, enables the three inches of emitter periphery to be placed in the 0.0192 square inch area stipulated by the thermal dissipation requirements of the contract.

Three different emitter designs were proposed to meet the requirement of collector area and emitter periphery. Each design involved some variation in processing techniques. The designs are discussed in detail in section III-C (Surface Geometry).

10. Switching Times

Of the four switching times: τ delay, τ rise, τ storage and τ fall, only the storage time is of major importance in limiting the switching speed of the device. The delay time is less than 20 nanoseconds and the rise and fall times are in the 80 nanosecond range. Therefore, attention will be focused on the storage time.

It is reasonable to assume that under steady-state conditions the base current is used only to supply recombination current. The charge stored in the base can then be related to the minority carrier life time and base current by $Q = I_B\tau$. When the transistor is operating in the active region, the base current, $\frac{I_C}{h_{FE}}$, stores charge

$$Q_A = \frac{I_C}{h_{FE}}\tau \text{ coulombs in the base} \quad \ldots\ldots\ldots\ldots\ldots\ldots (10)$$

When the transistor operates in the saturation region, the base current I_{B_1} stores charge

$$Q_S = I_{B_1}\tau \text{ in the base} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (11)$$

The difference between Q_S and Q_A is the excess charge Q_X which must be removed from the base by I_{B_2} during the storage time.

Therefore, $$Q_X = \left(I_{B_1} - \frac{I_C}{h_{FE}}\right)\tau \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (12)$$

In this case I_B = 2A

I_C = 20A

h_{FE} = 25

$\tau = 0.2 \times 10^{-6}$ sec.

Therefore $Q_X = 0.2\mu$ coulombs.

In device structures where the base is more highly doped than the collector, the base will have a high injection efficiency into the collector when that junction is forward biased. The charge stored in the undiffused collector material will be appreciable because the width of the undiffused region required to achieve high collector breakdown voltage is 8 times greater than the base width. In this case, the charge stored in the collector may be approximated by:

$$Q_c = \frac{a^2 \gamma I_C}{2 D_p} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (13)$$

where a is the undiffused collector region thickness = 1.07×10^{-3}cm,

D_p is the diffusion constant for holes in silicon under high injection = 26 cm^2/sec,

I_C is the collector current = 20 amperes, and

γ is the base injection efficiency into the collector = 0.75

An equation for storage time has been expressed by Phillips[7] which

can be stated as:

$$\tau_s = \left(\frac{Q_A}{I_E} + \frac{Q_C}{I_C}\right) \ln \left[\frac{I_{B_1} - I_{B_2}}{\frac{I_C}{h_{FE}} - I_{B_1}}\right] \quad \ldots\ldots\ldots\ldots (14)$$

Since $\beta_F = \frac{I_C}{I_{B_1}}$, $\beta_N = h_{FE}$ and $I_{B_2} = -I_{B_1}$; the log term can be simplified and the expression can be related to device geometry as:

$$\tau_s = \frac{W^2}{2D_n} + \frac{a^2}{2D_p} \ln \left[\frac{2}{\frac{\beta_F}{\beta_N} + 1}\right] \quad \ldots\ldots\ldots\ldots\ldots (15)$$

In this case $\frac{W^2}{2D_n} = 2.1$ n sec.

$$\frac{a^2}{2D_p} = 79 \text{ n sec.}$$

and $$\ln \frac{2}{\frac{\beta_F}{\beta_N} + 1} = 0.54$$

then $\tau_s = 44$ n sec.

It can be seen from the results of this calculation that the thickness of the collector region should be kept as small as possible. The current gain (β_N) should also be kept down because the wider base width necessary to achieve this does not seriously increase the total storage time.

B. PROCESS DESIGN

1. Diffusion

The collector-base and emitter-base junctions are formed by diffusing n and p-type material through areas defined by oxide masking techniques. Throughout the device design section of this report, reference has been made to the values obtained for the impurity profiles of these junction diffusions. The concentrations, junction depths and junction gradients are determined by time, temperature and surface concentration of the diffusants. The base diffusion is performed first, using boron as the p-type source. The emitter diffusion, using phosphorus as the n-type material, follows.

The base diffusion process is performed in three steps. Initially, boron is deposited at 900°C for 1 hour in a closed box system. This deposition results in a high surface concentration, and shallow penetration. The depth is determined by an erfc relationship which relates the parameters in the following manner.

$$C(x) = C_o \operatorname{erfc} \frac{X}{2 (Dt)^{1/2}} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (16)$$

where D is the diffusion constant at 900°C = 7×10^{-15} cm^2/sec, (8)

t is time = 1 hour,

X is the junction depth,

C_o is the surface concentration, and

C(x) is the concentration at a distance of x from the surface.

The thickness of the deposited layer determined by this relationship is approximately 0.01 mil.

The boron is then diffused into the silicon at 1200°C for 2 hours, in the absence of a boron source. The solution of the differential equation of a diffusion without a constant surface concentration is a Gaussian distribution. The relationship is

$$C(x) = C_o e^{-x^2/4D_t} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (17)$$

and solving for D yields

$$D = 3.2 \times 10^{-12} \text{ cm}^2/\text{sec.}$$

Although the diffusion time is only twice that of the deposition time, the depth is much greater because the diffusion constant has increased 500 times due to the 300°C increase in temperature. Fuller and Ditzenberg[8] have shown the diffusion constant of both boron and phosphorus to change exponentially with temperature.

$$D = D_o e^{-\Delta H/RT} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (18)$$

where D is the diffusion constant at temperature I,

D_o is the initial diffusion constant = 10.5,

ΔH is the enthalpy of diffusion = .85000 cal/mol,

R = 1.987 cal/mol, and

T is temperature in °K.

The third step in the base diffusion is the added penetration resulting from the emitter diffusion. This operation is very short and is done at a lower temperature than the boron diffusion. The often observed "push-out" effect occurs here and results in an increase in the collector junction depth.

The parameters governing the emitter diffusion are adjusted to provide for a heavy n-type concentration and a specific base width. The emitter

diffusion is performed in a one-step operation in the presence of a phosphorus atmosphere. Therefore, the surface concentration remains constant at a value determined by the equilibrium solid solubility of phosphorus in silicon, throughout the diffusion operation. The boundary values of this diffusion operation yield an erfc solution of the differential equation, resulting in the same relationship as shown in equation (17).

In order to diffuse to a depth of approximately 0.1 mil, the optimum conditions appear to be a temperature of 1100°C for 10 minutes, which yields a surface concentration of 3×10^{21} atoms/cc and a diffusion constant of $4 \times 10^{-13} cm^2/sec$ [8]. Figure 6 illustrates the relationships of diffusion depth versus diffusant concentration, including the collector contact diffusion. Table III summarizes the diffusion relationships.

TABLE III

SUMMARY OF DIFFUSION RELATIONSHIPS

Diffusant	Step	Temp. (°C)	Time (min)	Diff. Const.	Surface Conc.		Junction Depth
					Initial	Final	
Boron	Dep.	900	60	7×10^{-15}	3×10^{20}	—	—
Boron	Diff. I	1200	120	3.2×10^{-12}	—	—	—
Boron	Diff. II	1100	10	4×10^{-13}	—	7×10^{17}	0.19
Phosphorus	Dep.	1100	10	4×10^{-13}	3×10^{21}	3×10^{21}	0.10

2. Metallizing

Having established that the emitter injection efficiency is dependent on the periphery of the emitter rather than the area, it is obvious that the emitter should be designed with surface dimensions that

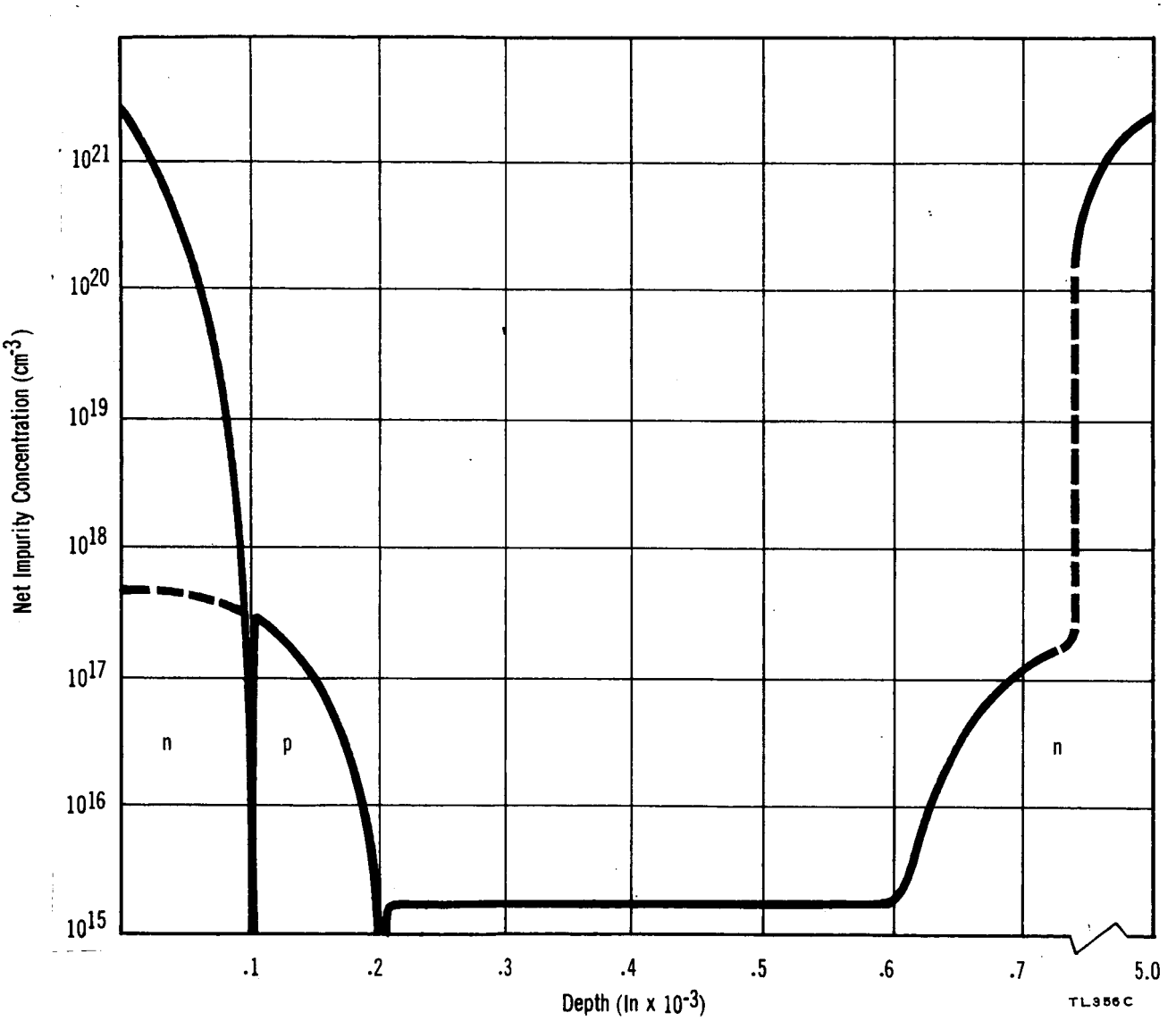


FIGURE 6 TA2438 IMPURITY PROFILE

result in the longest emitter edge for a given emitter area. A pattern which utilizes narrow, long fingers will achieve this end. In the interdigitated type pattern used for the TA 2438 (see Figure 7), the maximum length for a finger of a specific width is determined by the voltage drop obtained when current is conducted down the finger. The loss in potential, due to the voltage drop in the finger, results in a reduced bias at the emitter-base junction as a function of finger length.

The equation:

$$I = I_o \quad e^{\frac{(V_J)q}{kT}} - 1 \qquad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (19)$$

where I is the current,

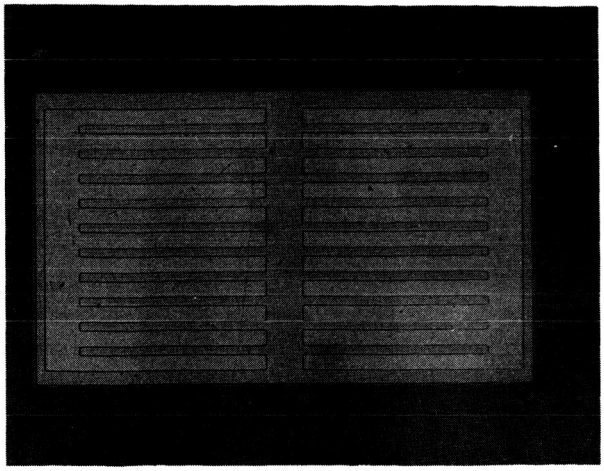
I_o is the constant,

V_J is the voltage across the junction, and

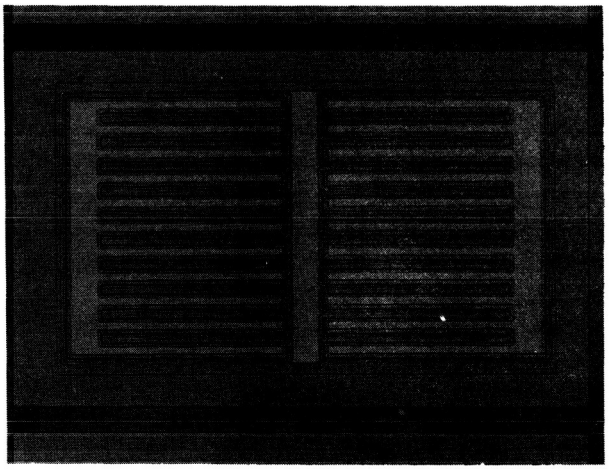
$\frac{kT}{q}$ = .026 Volts at 300°K and .042 Volts at 473°K

shows that injection from the emitter is exponentially dependent on the potential across the junction. A drop in V_J of kT/q volts from one end of a finger to the bond area results in a reduction factor of 1/e in emitted current. Therefore, it is desirable to keep the voltage drop along the finger below this value.

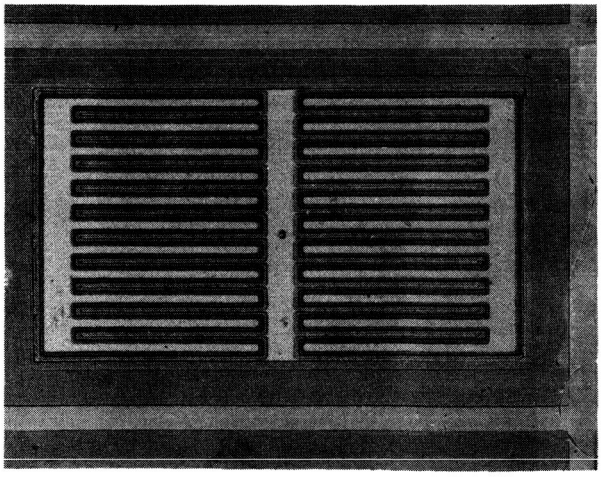
The metal used to contact the emitter is aluminum. Pattern definition of the metal and other design criteria have suggested a contact area of 3 mils in width. The length of a finger on the TA2438 is 70 mils. Assuming perfect contact between the silicon and



a. Emitter Pattern



b. Metal Contact Pattern



c. Metallized Unit

FIGURE 7 TA2438 EMITTER PATTERN, METAL CONTACT PATTERN AND METALLIZED UNIT

the aluminum, the thickness of aluminum required to limit the voltage drop to kT/q, at the maximum operating current of 20 amperes and an h_{FE} of 10 can be calculated. The results of the calculation are based on the following design criteria:

a) The current/finger is 0.91 amperes in each of the 22 fingers.

b) The unit is operating at 200°C.

c) The aluminum is defined with an etch factor of one.

d) The voltage drop in the base finger tends to make the emitter-base junction more equipotential, thereby allowing the overall voltage drop in the emitter to be greater. At 2 amperes base current, the voltage drop in the .001" wide base finger is 1/3 that of the emitter. Therefore, allowable voltage drop in the emitter is:

$$V_{ef} = .042 + \frac{(.042)}{3} = .056 \text{ V.}$$

e) The cross-sectional area of the aluminum is a trapezoid with a 45° angle, having an area:

$$A_e = Wt - t^2 \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (20)$$

where W is the width of the finger = .003" and

t is the thickness of aluminum.

The expression used to calculate the metallizing thickness is as follows:

$$V_{ef} = \rho_{al} \frac{l_e}{A_e} \frac{I_{ef}}{2} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (21)$$

where V_{ef} is the voltage drop in an emitter finger = .056V and

ρ_{al} is the resistivity at 200°C = 1.92×10^{-6} Ω-in.

I_{ef} is the emitter current/finger = 0.91 amperes

and solving for t yields

$$.056 = \frac{1.92 \times 10^{-6} \times 7 \times 10^{-2}}{3 \times 10^{-3} t - t^2} \times \frac{9.1 \times 10^{-1}}{2}$$

$$t = 0.42 \times 10^{-3} \text{ in.} \approx 100{,}000\text{Å}$$

This is the thickness of aluminum that was evaporated on the wafers.

C. SURFACE GEOMETRY CONSIDERATIONS

The design parameters that have been determined thus far have not completely specified a surface configuration. The design of this configuration can help to optimize the electrical parameters of the device.

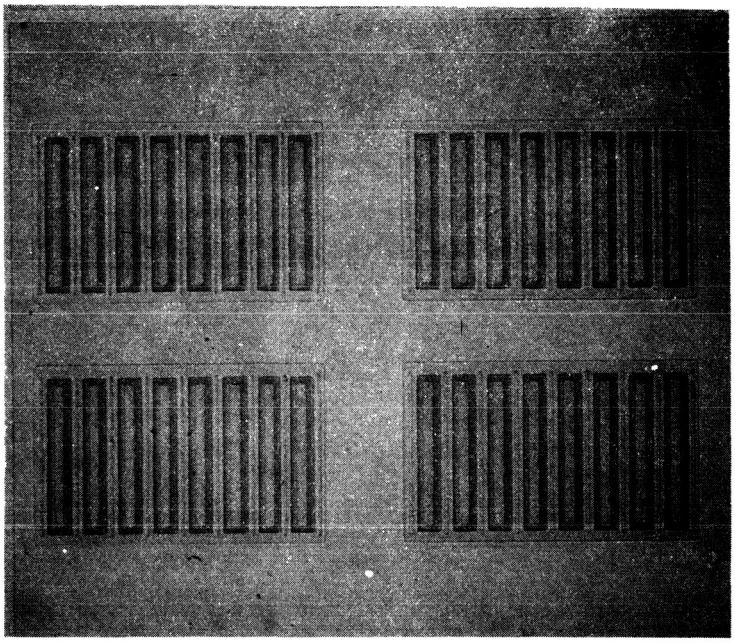
The original contract proposal indicated that the unit would be made as either a mesa or planar version of the TA2089 (now called TA2438). This transistor (see Figure 6) is an interdigitated or comb type unit. It has 2 emitter areas with a base bonding area between them. The emitter has two 10 x 100 mil bonding areas with 11 fingers coming from each of the bonding areas. The base has one 10 x 100 mil bonding area with 12 narrower fingers attached on each side of the bonding area and positioned between the emitter fingers. The collector-base junction is a rectangle with a 19,200 mils^2 area.

Minimizing the collector and emitter area, while maintaining a constant emitter periphery, is an improvement that would be advantageous for several reasons. It would increase the speed of transient characteristics, such as frequency response and switching time, while maintaining the same current handling capability. Diffusion studies have shown that the planar diffusion yield decreases exponentially with an increasing

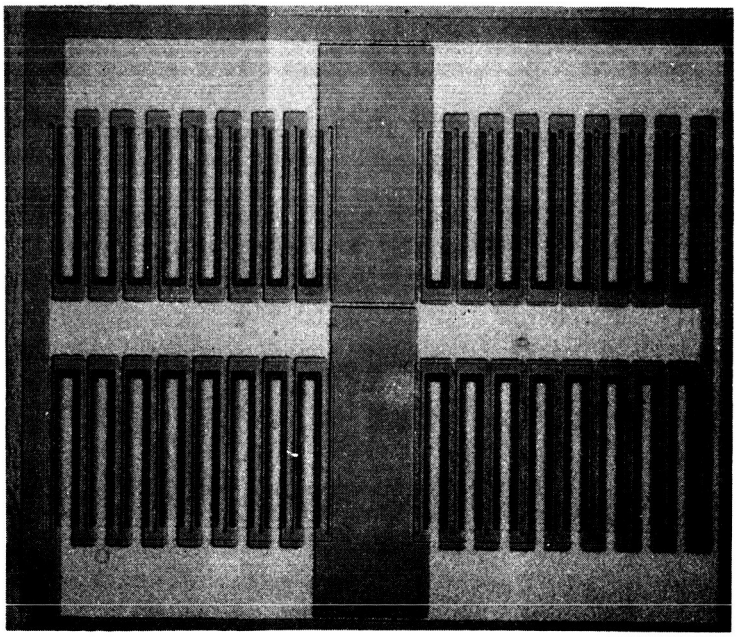
base area. If thermal resistance requirements permit, a decrease in collector area could also result in a decrease in pellet area, thereby increasing the amount of pellets on a wafer. This increase in pellets would result in a reduction in manufacturing costs.

The simplest way to reduce base area, aside from decreasing tolerances, is to move the bonding area out of the base area. The bonding area contributes very little to the active area of the device. This could be done by placing the metal bonding areas on the oxide which covers the collector. The TA2379 (see Figure 8) was designed for this purpose. The pellet area remained approximately the same as that for the TA2089, however, four discrete base areas were incorporated. Each of the base areas contained nine emitter stripes. The isolated emitter stripes and base stripes are connected by defining a comb type metal pattern which extends onto the oxide over the junction.

A more radical design concept was employed in the TA2306 pattern. In addition to reducing the collector area to emitter periphery ratio, voltage drops along the emitter fingers were virtually eliminated, resulting in evenly distributed injection. This was accomplished by the "overlay" technique,in which the emitter metallizing is a sheet passing over the base finger metallizing (see Figure 9). The base metal is insulated from the emitter sheet by a thin film which coats the metal everywhere except the bonding areas. This design was produced mainly to provide a feasibility study of this approach. RCA device design engineers feel that the success of this structure could be a major advancement towards increasing the performance of high power, high speed transistors.



a. Pattern Prior to Metallizing



b. After Metallizing

FIGURE 8 TA2379 METALLIZING

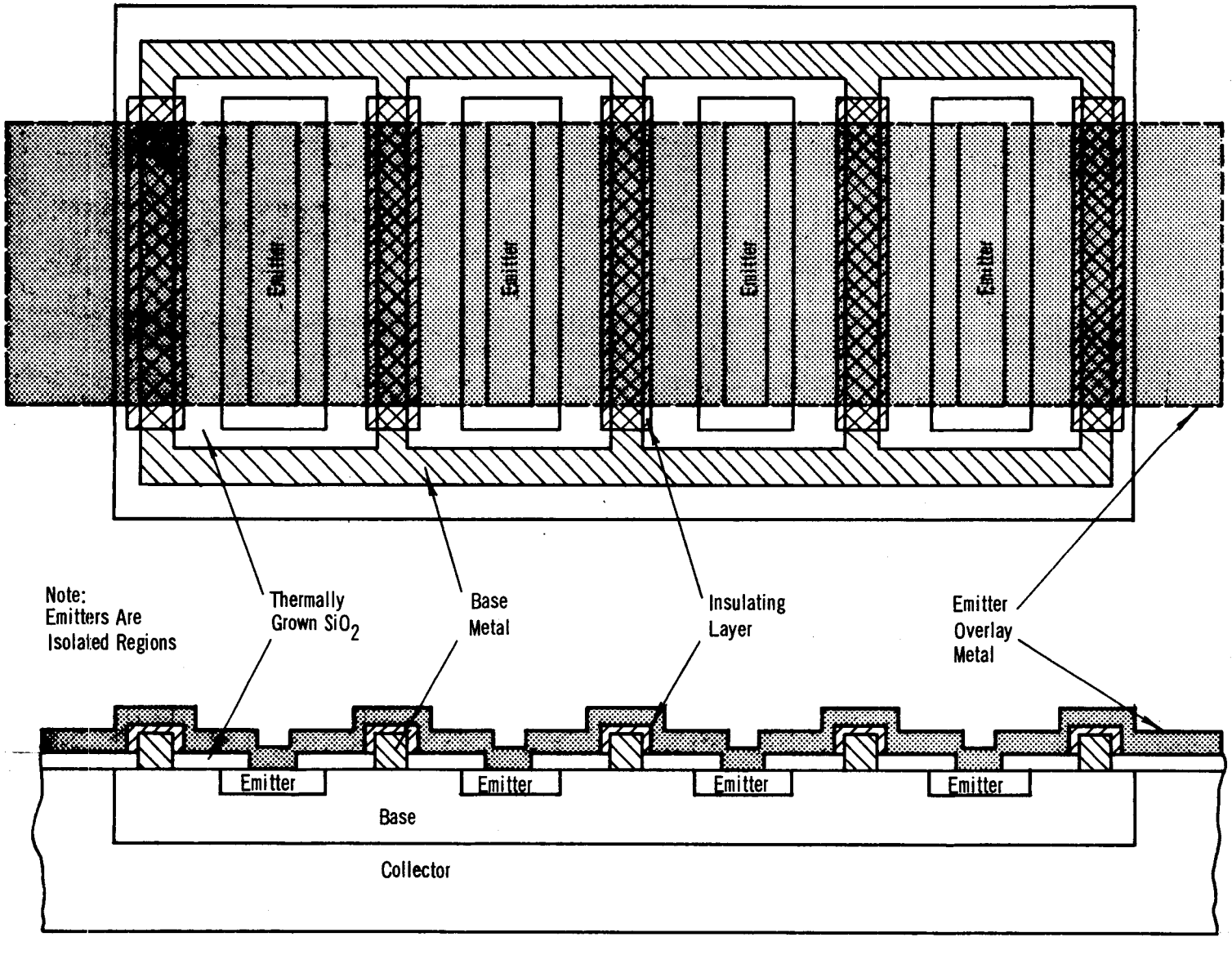


FIGURE 9 TA2306 OVERLAY TRANSISTOR

A comparison of surface dimensions of this unit to the two alternate devices is shown in Table IV.

The problems entailed in processing these two new designs (TA2306, TA2379) combined with the fact that contract requirements could be met using the more conventional planar TA2438 were the factors which dictated the final design approach. The specific processing difficulties for the TA2379 and the TA2306 devices are detailed in sections V-A3 and V-A4 respectively.

The TA2379 was not used for two reasons. The first reason was that improvements in diffusion yield resulted in the relationship of diffusion yield to base area to be reduced, therefore eliminating the differences in yield between the TA2438 and 2379. The other reason was that high reverse leakage currents resulted from aluminum metallizing on the oxide over the junctions.

The problems encountered in the fabrication of the insulating layer was the major cause for abandoning the "overlay" TA2306. Although some pellets were made with transistor characteristics which proved the feasibility of the technique, it was felt that there were too many problems still associated with the process.

The planar TA2089 (now called TA2438) rather than the mesa version was selected because of the obvious advantages of reliability and reproducibility of product, obtainable with the planar structures.

TABLE IV

COMPARISON OF TA2438, 2379 and 2306 SURFACE GEOMETRIES

Device	Emitter Length, L_e (inches)	Collector-Base Area, A_c (inches^2)	Emitter Area, A_e (inches^2)	$\frac{A_c}{A_e}$	$\frac{A_c}{L_e}$ (mils)	$\frac{A_e}{L_e}$ (mils)
TA2306	3.30	0.0137	0.00500	2.74	4.15	1.51
TA2379	2.56	0.0138	0.00384	3.60	5.40	1.50
TA2438	3.20	0.0192	0.01150	1.67	6.00	3.60

IV. DEVICE FABRICATION PROCESS

A. INTRODUCTION

The basic planar process is well known and has been widely reported. Many types of silicon devices have been fabricated using this technology. The process consists of a series of distinct operations with each operation demanding its own scientific disciplines.

As the performance demands of the transistor are increased, the fabrication process becomes more intricate. This in turn, tightens the tolerances and exposes the limitations of the individual operations. The end result is a more stringent control of process variables and new process developments. Thus, each operation of the planar process is eventually tailored to the specific family of devices to be fabricated.

A detailed description of the planar process that was evolved for the fabrication of a transistor, which meets all of the requirements of this contract, will be presented in this section. This description will follow the normal processing sequence, from diffusion through packaging.

The device, which is basically an NPN triple diffused device with a planar structure and oxide passivated surface, is processed through vapor diffusions, photoresist operations and metal contacting operations in wafer form. The wafers are then scribed into pellets, metallurgically mounted into an isolated collector package, thermocompression bonded and sealed by means of a cold weld.

B. COLLECTOR DIFFUSION

The raw silicon material, in wafer form (one-inch in diameter), is lapped to a 0.015 inch thickness. This material is n-type with 3 to 4 ohm-cm resistivity.

Collector diffusion is a two-step operation. Phosphorus is deposited on both sides of each wafer at 1250°. Control of impurity concentration is monitored with p-type wafers. The phosphorus silicate glass formed during this deposition step is removed with hydrofluoric acid and sheet resistance measurements are taken on the p-type control samples, using a four point probe. The wafers are then diffused for 140 hours. Sheet resistance measurements and depth of penetration measurements are made on the p-type control wafers.

This diffusion yields a Gaussian impurity distribution with an impurity concentration at the surface of about 6.0×10^{20} phosphorus atoms per cm^3 and a depth of penetration of about 0.005 inch.

One side of each wafer is then lapped to remove all of the diffused phosphorus, exposing the original 3 to 4 ohm-cm material. The wafer is then polished to an optically-flat and scratch-free finish by mechanical and chemical polishing techniques. This insures subsequent formation of flat and parallel base and emitter junctions and also provides a flat surface which is needed to maintain the critical geometry tolerances of the transistor.

The initial oxide is then grown and used as a selective area mask

against diffusion of boron in subsequent steps. The wafers are now ready for base area definition.

C. BASE PHOTORESIST

The wafers are covered with Kodak Photoresist (KPR) and spun on a central whirler. Thus a KPR coating approximately 2000-5000Å thick is formed on each wafer. At this point, the wafers are ready for pattern masking. The important criteria for base pattern masking is a completely opaque mask and good definition. Base masks must be continually checked for pinholes and other imperfections that might cause electrical failures in the completed device.

After the base pattern is exposed, developed, dried, and baked, a hydrogen fluoride system is used to etch the silicon dioxide window that was defined in the photoresist. Each wafer is inspected at 150x magnification to determine if oxide residues have remained in the base.

The photoresist is then removed and the wafer is cleaned.

D. BASE DIFFUSION

Base diffusion is a two-step process. Boron impurities are deposited in the base areas of each wafer using a boron box technique. Sheet resistance measurements are made on control wafers to monitor the boron impurity concentration at the surface. In the second stage, the boron impurities are diffused deeper into the wafer surface. Sheet resistance measurements and impurity penetration measurements are again made on control wafers.

This diffusion forms isolated, rectangular regions, which are doped with boron. The boron concentration at the surface is 8.0×10^{17} atoms per cm^3 and follows a Gaussion distribution. During the base diffusion, a new oxide is grown over the entire wafer in preparation for the emitter area photoengraving.

E. EMITTER PHOTORESIST

The purpose of the emitter photoresist operation is to create openings in the base oxide where the emitter diffusion will occur. There are two requirements which make this operation complicated. These requirements are the incorporation of a registration step and the absence of pinholes or voids in the photoresist mask.

The preconditioning of the oxidized wafer is the same as that for the base pattern definition. After the wafer is preconditioned, it is coated with a 5000 Å thick photoresist film.

The alignment system (see Figure 10) is composed of a NIKON comparator and a specially designed alignment fixture. This alignment system, combined with ease of viewing on the 24-inch diameter Nikon screen, reduces operator strain considerably, thereby enhancing the reliability of a completely operator-dependent system.

After the wafer is aligned, exposure is accomplished with a high pressure lamp utilizing the optics of the Nikon system. This arrangement reduces the possibility of misalignment,in that the alignment system need not be moved. The development of the photoresist film is performed in a 3-stage KPR developer system in order to reduce surface residues.

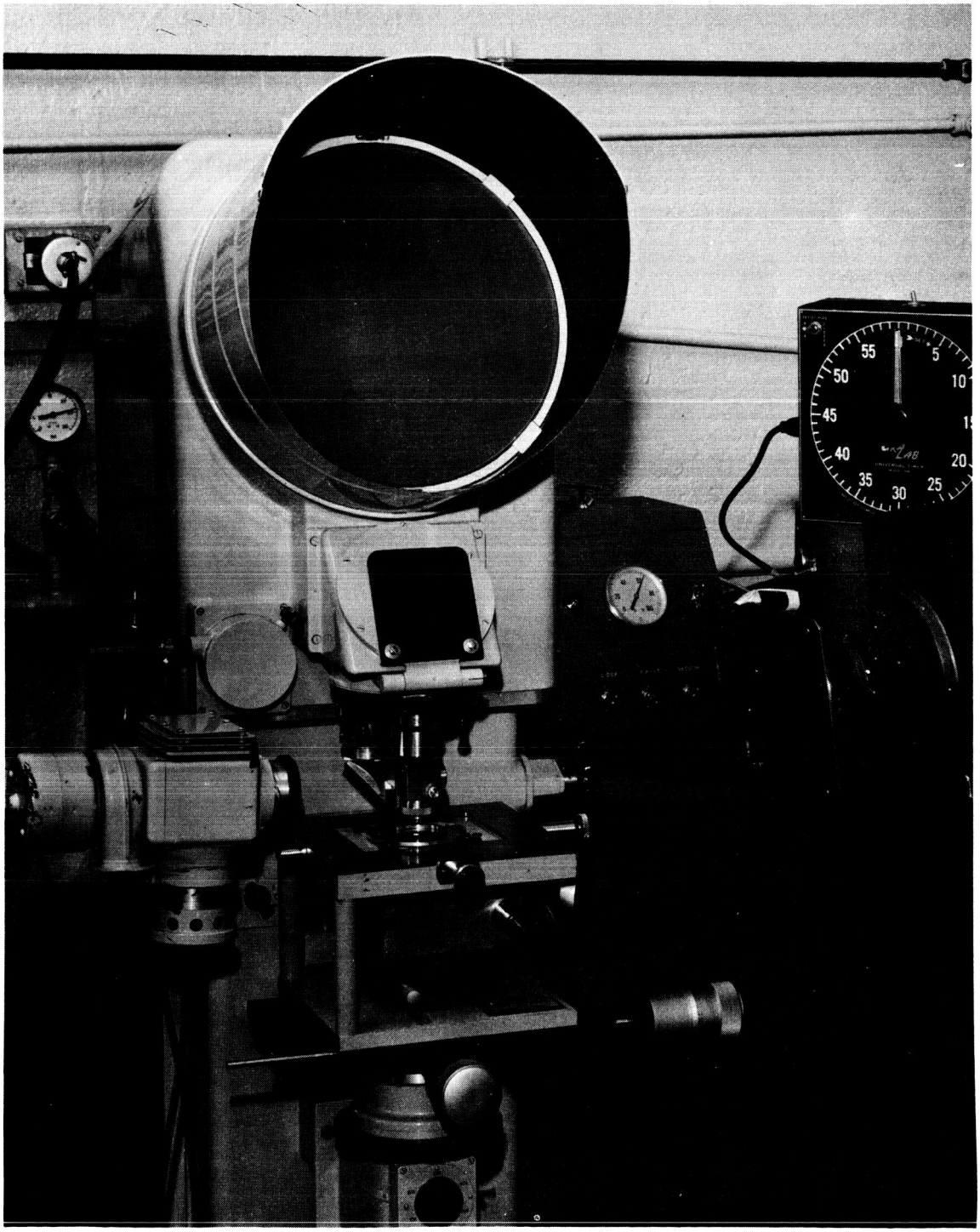


FIGURE 10 PHOTORESIST ALIGNMENT AND EXPOSURE SYSTEM

Etching is performed with a buffered oxide etch. The etching cycle is rigidly controlled (i.e., etching is stopped immediately after all the oxide is removed) to minimize the incidence of etched "pinholes" in the oxide in areas other than the emitter region.

After the emitter "windows" in the oxide are etched, the photoresist is stripped in the standard manner. The emitter pattern is inspected to determine the amount and type of residues and voids remaining in the oxide. The wafers are then subjected to a post photoresist clean-up.

F. EMITTER DIFFUSION

Emitter diffusion is a one-step process,using phosphorus as the diffusant. Surface concentration measurements and junction penetration measurements are made on p-type control wafers.

The impurity distribution is a complimentary error function type which forms a p-n junction in the base at a penetration of about .000070 inch.

After checking the collector emitter breakdown voltage, the wafers are returned to the furnace for a final oxidation.

G. CONTACT PATTERN PHOTORESIST

The photoresist operation which follows emitter diffusion serves a different purpose than the previous diffusion masking operations. This operation is performed so that the oxide over the emitter and base areas can be opened to prepare for the subsequent formation of metallic ohmic contacts. The photoresist problems entailed in accomplishing this are quite

similar to those encountered in the definition of the emitter pattern.

Processing wafers through the contact pattern photoresist operation is identical to the emitter pattern photoresist operation. The wafers are registered and exposed on the Nikon alignment fixture, using the mask for metallic contact openings. The development of the image is accomplished in the previously described multi-stage system. The etch time is again kept to a minimum. The wafers are stripped of photoresist, inspected and cleaned again as in the normal photoresist procedures.

After the contact pattern photoresist operation is completed, the first real electrical testing of the units, in wafer form, is performed. Yield data is taken and correlated to other diffusion data.

H. METALLIZING - ALUMINUM

The wafers that pass post-diffusion testing are ready for metal contacting. The purpose of metal contacting is essentially to produce a low resistance electrical path between the active junction area and the three external leads of the packaged transistor. Therefore, the requirements for transistor metallizing are the same as those for any other passive electrical connector. These requirements are:

1) Ohmic contact between the materials that it connects.
2) Lowest possible voltage drops within the body of the contacting metal.
3) Electrical isolation of metals at different potentials.

Aluminum was chosen as the metallizing material because it appeared to possess the greatest potential for fulfilling the requirements of a good

metal contact. The prime reason for the selection of aluminum was that a low resistance ohmic connection can be made between aluminum and silicon through the eutetic alloy formed at 570°C. Aluminum can be applied to a silicon surface by vacuum evaporation (a widely reported industrial technique), which is an excellent manufacturing operation for small parts.

Prior to evaporation, the wafers are surface cleaned. Two tungsten coils are placed in the evaporator and each is loaded with sufficient aluminum to evaporate 40,000Å. The cleaned wafers are placed two-inches away from the two coils. The system is then evacuated to the final evaporation pressure of 10^{-6} torr. Each coil is evaporated separately at 5-minute intervals. The final thickness of aluminum should be 80,000 to 100,000Å, as determined by the design considerations. The wafers are immediately transferred to the photoresist area where they are coated with KPR.

I. METAL DEFINITION

The ability to define thick aluminum films to close tolerances is of great importance in determining design criteria of planar transistors. Metal definition governs r_{bb}' and the ratio of emitter area to emitter periphery, both of which should be kept as low as possible for optimum performance. The ability to define 10μ-thick aluminum films with an etch factor of one permits much greater flexibility in the optimization of transistor parameters.

The technique used for defining the aluminum pattern is a photoresist

masking procedure combined with etching of the metal. After coating with KPR, the wafer is dried in a moisture-free system for one hour and then registered and exposed on the standard alignment-exposure system. The image is developed in KPR developer which incorporates a series of containers to minimize formation of residues. The aluminum pattern is defined by chemically removing the excess metal.

J. ALLOYING

The electrical contact made between the evaporated aluminum film and the silicon surface after evaporation is non-ohmic. A heat treatment is necessary to lower this contact resistance, however, it is not necessary to heat the wafers to the aluminum-silicon eutectic temperature to achieve the ohmic contact, since surface alloying occurs at temperatures ranging from 500 to 570°C.

Prior to heat treating, the wafers are cleaned to remove surface contaminants. The wafers are placed in a clean quartz boat and inserted into the hot zone of a nitrogen flushed open-tube furnace. The wafers are then cooled in dry nitrogen. Finally, the wafers are electrically tested for contact resistance and reverse current characteristics.

K. SCRIBING

The alloying operation concludes the processing of the transistor in wafer form. At this point, the wafer is pelletized by a scribing and breaking operation which incorporates an RCA designed scriber.

The scribing operation incorporates a moveable microscope, a vacuum plate

capable of rotary motion and X and Y movement. Actual scribing is performed by a diamond point that traverses the wafer.

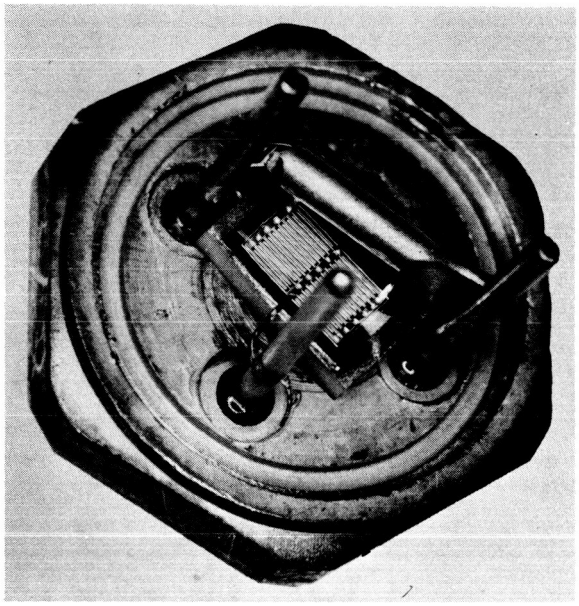
L. PACKAGING

The aim of packaging the transistor is twofold. One aim is to protect the fragile silicon pellet from both physical and environmental abuse. The other is to provide terminals for connecting the unit to other parts of the circuit. As a corollary to the second aim, the case must also provide good thermal dissipation characteristics, thus enabling the device to operate at maximum power level.

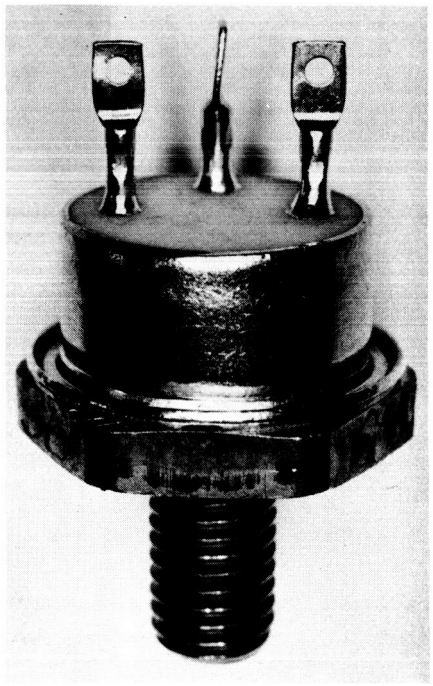
To meet the two aims, an isolated collector 11/16" DES package (see Figure 11) was designed. In this configuration, the leads offer low resistance and are electrically isolated from the case. After the assembly is metal plated, a beryllium oxide disc is alloyed to the surface with lead solder. The joints are then inspected to insure complete wetting.

M. MOUNTING

The pellet is alloyed to the beryllium oxide metallizing in the furnace shown in Figure 12. This furnace has a water-cooled base plate with a nitrogen inlet and two power terminals extending through the center. The heating element, a monel strip, connects the two terminals. A hole is located in the center of the strip to hold the stud. The system is encased in a one-piece cylindrical pyrex top, connected to the base plate with an O-ring seal. A one-half inch diameter hole in the pyrex wall permits entrance of piece parts and the rod used for agitation.



a. Unsealed



b. Sealed

FIGURE 11 ISOLATED COLLECTOR 11/16" DES PACKAGE

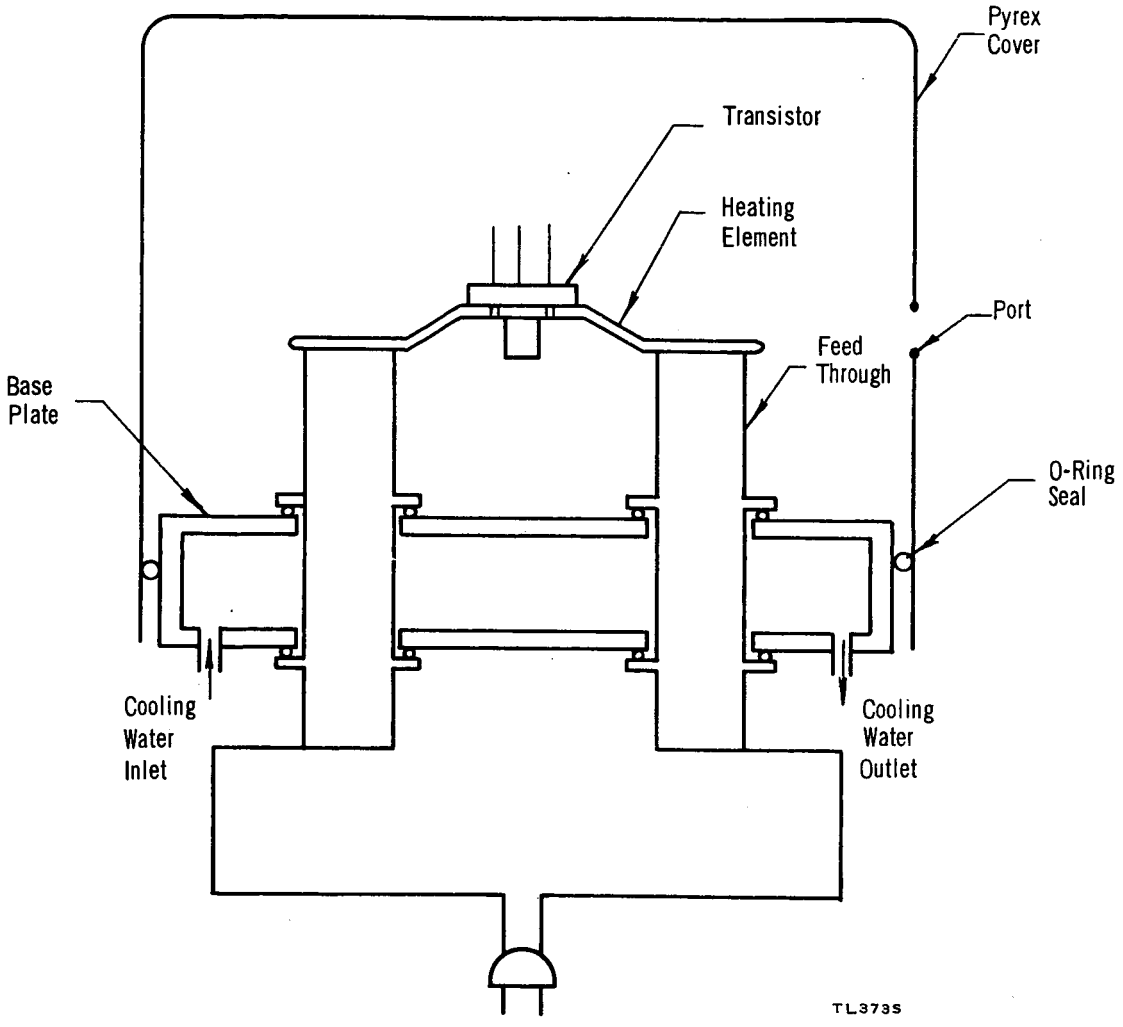


FIGURE 12 PELLET MOUNTING FURNACE

The stud, with beryllium oxide mounted to it, is placed in the furnace, and flushed with nitrogen. A gold-silicon preform is placed on the beryllium oxide piece and the system is heated to melt the solder. The pellet, which was rinsed in acetone and dried prior to this step, is then placed in the furnace and alloyed to the beryllia. Pellets are periodically lifted from the beryllium oxide to check that the back of the pellet is completely wet by the solder.

A gold collector connector wire with a 5 mil x 30 mil cross section is alloyed to the top of the beryllia during pellet mounting. The system is then cooled to room temperature. The complete mounting operation takes about 7 minutes, 5 of which are at elevated temperature. The units are probed once again for electrical characteristics with specific attention paid to degradation of junction characteristics.

N. BONDING

The units are bonded to provide a low resistance electrical connection between emitter and base metallizing and the external leads. Gold wire, is used for this purpose. The wire is thermocompression bonded in six places along the back of the metallized comb (one wire for the base and one wire for each of the two emitter sides) and then welded to the leads. The units are then cooled to room temperature. The bonding equipment used is a Kulicke and Soffa Type 402 Bonder. The bonder incorporates a heater column which was designed for this particular package.

After the gold wire is attached, a copper-cored kovar bar is welded perpendicularly to the emitter lead. The bar extends over the unit, passing

directly above both emitter combs. The bonding wires are then welded to the appropriate terminals. The emitter wires from each comb are welded to the post directly above them, thereby lowering the series resistance of the emitter connections. The collector and base wires are both welded to their posts (see Figure 11a).

High power tests such as 20-ampere current gain, saturation voltage, and thermal resistance with switching speed are performed on the bonded units. The yield at this point is recorded and only acceptable units are sent to sealing.

O. SEALING

One of the major advantages of planar, oxide passivated devices is that a minimum of surface treatment is required for sealing. Prior to sealing, the units are checked for seal ring defects, bonding defects, cap size, and other physical criteria that might hinder either device performance or the ability to seal.

The units are individually sealed by cold welding with a Denison Hydraulic Multipress equipped with an enclosure filled with a dry nitrogen ambient. After sealing, the three therminals of the cap are crimped to insure good ohmic contact to the encased terminals (see Figure 11b).

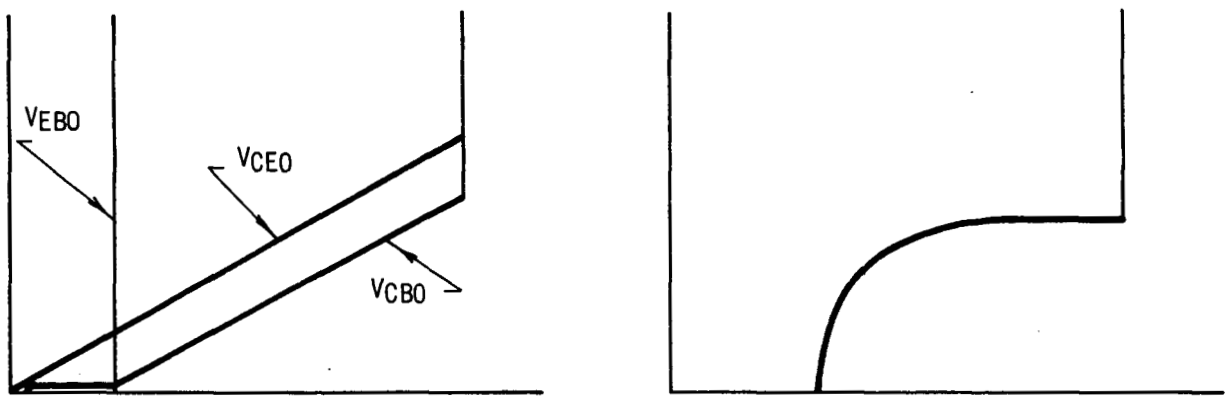
V. PROCESS ADVANCEMENTS

A. PELLET PROCESSING

1. Diffusion

At the beginning of this program, it was doubtful that this transistor could be made with the planar geometry. At that time, no large area planar device had been made. Because of the experience developed with small area transistors, difficulties were anticipated. However, it was felt that the planar geometry was necessary for reliability reasons and, therefore, a considerable effort was made to solve the problems involved.

One of the most severe problems encountered in the fabrication of large area planar transistors is manifested in their reverse biased junction characteristics. Figure 13a shows the V_{CEO}, V_{CBO}, and V_{EBO} of a transistor with such a failure mechanism. The V_{CEO} parameter shows a high current resistive path from the emitter to the collector. This path extends from the emitter vertically through the base into the collector. Inversion layers or channels across the surface of the base are ruled out because their vertical paths or "pipes" have been identified and when etched the units recover. In some cases, the pipe pinches off as the base-collector diode is reverse biased. In such cases, the V_{CBO} parameter appears as shown in Figure 13b. Whether V_{CBO} appears as shown, depends on the diameter of the pipes and the number of pipes in the unit. Most of the first large area transistors made had such a large number of pipes that the pinchoff



a. Pipe Effect

b. Pipes With Pinch-off Effect

TL377C

FIGURE 13 V-I CHARACTERISTICS OF PLANAR DIFFUSION FAILURES

phenomenon was not evident. It has been found that these pipes are caused in various ways. Gotzberger has shown that pipes are formed by diffusion of localized spots of phosphorus or other substances.[9] A thorough cleaning procedure was developed, using double distilled deionized water and a desorption mixture, to reduce the occurrence of pipes of this nature to an insignificant level. Other pipes are formed when phosphorus is diffused into the wafer during the emitter junction formation. These pipes are of a more complicated nature and are a result of imperfections in the raw material.

Pipes in diffused junctions can be identifed by several methods. Cross-sections or angle laps can be made and if the density of pipes is high the probability of bringing one to the surface is good. The junction is then stained and the pipe is clearly defined as a round white spot which indicates n-type. Successive lappings of the same pipe will show that it penetrates the base into the collector region. Another technique is to reverse bias the base-collector diode (this must be done before the emitter has been diffused) and to examine the base area with a microscope. In this instance, the pipe appears as a small round light spot (microplasma) which brightens and dims with current. After the pipe is located with the reverse biased light spot technique, it is angle lapped to show that it penetrates through the base. Pipes which exist after base diffusion are those formed by the diffusion of spots of phosphorus or other impurities. The more troublesome

pipes, which occur during the emitter diffusion, cannot normally be located by observation of microplasmas, because they are covered by the emitter. It was found, however, that these pipes are formed when the wafers are subjected to phosphorus deposition and diffusion conditions, whether or not the oxide in the emitter area has been removed. By treating the wafers in this manner, without the emitter opening, it is an easy matter to identify the pipes by observation of light emission. If the wafers are protected with an evaporated silicon monoxide coating and processed in a phosphorus atmosphere, no pipes are formed.

It has been pointed out that pipes formed during the emitter diffusion constitute the most difficult problem encountered with the planar geometry. This has been proven by an experiment which shows that these pipes occur in the planar geometry and not in the mesa geometry. Therefore, these pipes are mainly responsible for the large difference in yields between large area planar and mesa structures. Three groups of wafers consisting of four wafers each and labeled A, B, and C were used in the experiment. The wafers were selected at random from a lot which had a diffused n^+ region approximately 4.5 mils thick and with a polished surface on the 3 to 4 ohm-cm side. The experiment incorporated the following six-step process:

Step 1: Group A and B had an initial oxide grown in steam at 1200°C for 15 minutes, as in normal planar processing. Group C had no initial oxide as in normal mesa processing.

Step 2: Group A was processed through a photoresist operation to form base areas as in normal planar processing. Group B was subjected to a hydrofluoric acid etch to remove all of the oxide. Group C had no treatment as in normal mesa processing.

Step 3: Groups A, B, and C were processed through base diffusion which is common to both mesa and planar processing. An oxide layer was grown over the entire wafer in this processing.

Step 4: Groups A, B, and C were processed through the emitter diffusion step, still covered with oxide.

Step 5: Group A had the oxide removed by hydrofluoric acid. Groups B and C were mesa etched to the same base area as Group A.

Step 6: Light spot counts were made on all of the units of each wafer in each of the groups.

A summary of the results of this experiment are shown in Table V. This data shows that the group processed without the initial oxidation step has an average pipe density of less than half that of the other two groups. Using $\ln y = -Na$, where: N is the pipe density, A is the area of the unit (0.01920 square inch), and y is yield; the yield for each group can be calculated as:

Group	Calculated Yield (in %)	Measured Yield (in %)
A	3.7	6.4
B	5.0	5.0
C	20.2	32.6

This is in good agreement with the yields determined from the percent

of units with light spots. If the pipe density obtained on the planar group is used to calculate the yield on the 2N1613 transistor (which has a base area of about 570 $mils^2$), the result would be 90.6 percent.

TABLE V

SUMMARY OF PIPE OCCURRENCE EXPERIMENT

Group	Wafer	No. of Units	Units with Light Spots (%)	Ave. No. of Light Spots Per Unit
A	1	14	85.8	2.00
A	2	13	100.0	3.77
A	3	15	93.4	3.87
A	4	5	100.0	1.80
	Total	47	93.6	3.3
B	1	13	92.3	5.23
B	2	12	100.0	5.50
B	3	9	89.0	4.34
B	4	5	100.0	24.4
	Total	39	95.0	7.6
C	1	12	66.6	1.75
C	2	12	58.3	.92
C	3	12	75.0	2.17
C	4	7	71.4	1.43
	Total	43	67.4	1.6

Group A = Thermally grown initial oxide, with Group B then processed as planar transistors.

Group B = Thermally grown initial oxide, which was removed in HF and then processed as mesa transistors.

Group C = No initial oxide, processed as mesa transistors.

All groups were diffused together, except during the initial oxide growth.

This points out the difficulty encountered in fabricating large area planar transistors versus small area devices.

The data developed from this experiment also shows that the processing for the initial oxidation results in a very large increase in pipe density. And, because these pipes are not present until after the emitter diffusion operation, two conditions must be satisfied. First, the oxide in the vicinity of the pipe must be easily penetrated by phosphorus and second, either the phosphorus diffusion is accelerated in the pipe or the boron atoms are depleted in the pipe. A possible explanation is that spiral dislocations absorb oxygen during the initial oxidation which then impedes boron diffusion and further oxidation in these areas. Because the possibility existed that the occurence of pipes was related to raw material, by spiral dislocation density or some unknown mechanism, an investigation was made into material obtained from different vendors. The results of this investigation will be discussed later.

With the knowledge that these pipes were formed during the emitter diffusion, a study was made of the occurence of pipes with regard to diffusion time and base width. This showed that the pipe density could be reduced by either decreasing the emitter diffusion time, increasing the base width, or both. It was also learned at this time that a larger base width was necessary for improved switching speed. The base width was increased from 0.070 mil to 0.10 mils and to maintain h_{FE}, the base surface concentration was lowered to 7×10^{17} atoms/cm^3. With these changes, the yields immediately improved

from 5 percent to about 20 percent. Material with the same specifications was purchased from four different vendors and processed. Table VI shows the results of this experiment, in the order in which the materials were processed. This experiment was conducted over a period of several months.

TABLE VI

RESULTS OF PROCESSING LOTS OF MATERIALS
PURCHASED FROM VARIOUS VENDORS

Lot	Vendor	Yield (%)
1	E	32.0
2	A	14.0
3	F	3.9
4	A	7.6
5	A	33.0
6	C	27.8
7	C	40.0
8	B	14.3
9	C	31.2
10	C	38.4
11	C	33.4
12	B	13.7
13	D	51.2
14	D	45.4
15	D	62.0

Material from vendor A seems to vary from very poor to good, from crystal to crystal. Material from vendors B, C and D is quite consistant and D gives yields of about 50 percent, which is excellent for this size device. It is evident from this experiment that the raw starting material plays an important role in processing large area planar transistors with high yields.

During the development of this device, several other interesting phenomena

were observed, which contribute to improved yields and are related to diffusion processing. It is quite common in planar transistor processing to have microplasmas on the base-collector junction periphery. Although this did occur occassionally in the TA 2438's processed, the problem posed was relatively easy to overcome. This phenomenon is caused by small particles of dirt, by ragged edges on the surrounding oxide and from photoresist pinholes in the oxide. The last two causes can be attributed to photoresist deficiencies, except that oxide growth during diffusion has some bearing on pinholes. It was found that pinhole counts, as determined by Cl_2 gas treatment, can be reduced by growing the oxides in steam and annealing them. Dirt particles, which collect very easily in the edges of the oxide, can be eliminated by very rigorous cleaning techniques, including the consistant use of a desorption mixture.

Any silicon diode, when reverse biased into avalanche, will emit light. The uniformity of the light is a measure of the quality of the diffusion. In well diffused devices, the entire base junction periphery emits light in a uniform line.

In processing a silicon diode, base-collector diode measurements made immediately after the base diffusion operation reveal that the junctions are leaky and have low breakdowns. This is due to metal precipitates and other impurities in the silicon and on the surface[10]. During the emitter diffusion, the phosphorus acts as a getter resulting in a sharp and much higher breakdown junction. The emitter diffusion processing was designed to best facilitate this gettering action compatible with the needs of the emitter junction.

2. Photoresist

Early in the program, it became apparent that one of the causes of low diffusion yields was an inadequate base photoresist technique. Some of the "pipes" associated with V_{CE} shorts and low collector-to-base breakdown voltage (V_{CB}) values, can be explained by oxide residues in the base area. These residues inhibit boron diffusion in local areas. The emitter diffusion may then overlap one of these areas into which boron was not diffused, that is, the n-emitter is on the n-collector. This overlapping results in a collector-to-emitter short.

The first attempt made to eliminate this problem consisted of placing stringent controls on the base mask handling procedure to minimize the effect of imperfections in the photoresist film caused by pinhole flaws in the masks. Photomasks were checked periodically and a record of their deterioration was maintained. However, this action did not completely eliminate the incidence of oxide that remained in the base area. Results of continued experiments into this problem revealed that the major source of residue in the base area was an inadequate developing procedure. As a result, developing procedures such as spray developing, the spinner technique and ultrasonic developing were investigated. A procedure eventually evolved which consisted of subjecting wafers to four KPR developer stages. The wafers were moved through the four stages in successively cleaner containers. Agitation was employed in the last stage. The developer was filtered each day, prior to use, and changed after every third

wafer was processed. Each wafer was subjected to a complete base area inspection after the pattern was etched. If an oxide residue appeared on more than three units on a wafer, the wafer was recycled through the photoresist process. However, recycling of a wafer occurred rather infrequently.

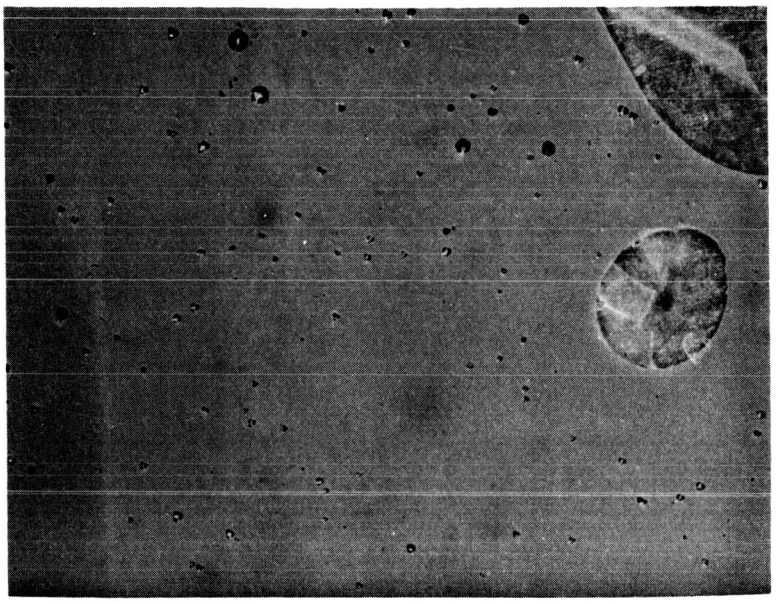
One of the basic problems associated with any surface coating process is the occurrence of voids in the film. This effect was initially encountered during the processing of TA2379 wafers, where emitter and base bonding areas were on the collector oxide. The voids in the photoresist resulted in the etching of holes into the collector oxide, which in turn resulted in collector-to-emitter and collector-to-base shorts.

Chlorine etching tests were performed on oxide layers that had been processed through the photoresist operation. Pinhole counts of the order of $1000/cm^2$ were obtained (see Figure 14a). The unexpectedly high pinhole density, obtained from this test, led to an explanation for another cause of low diffusion yields. The incidence of pinholes in the oxide, which covers the collector-to-base junction periphery, resulted in n^+ regions that shorted this junction during emitter diffusion. Applying the relationship

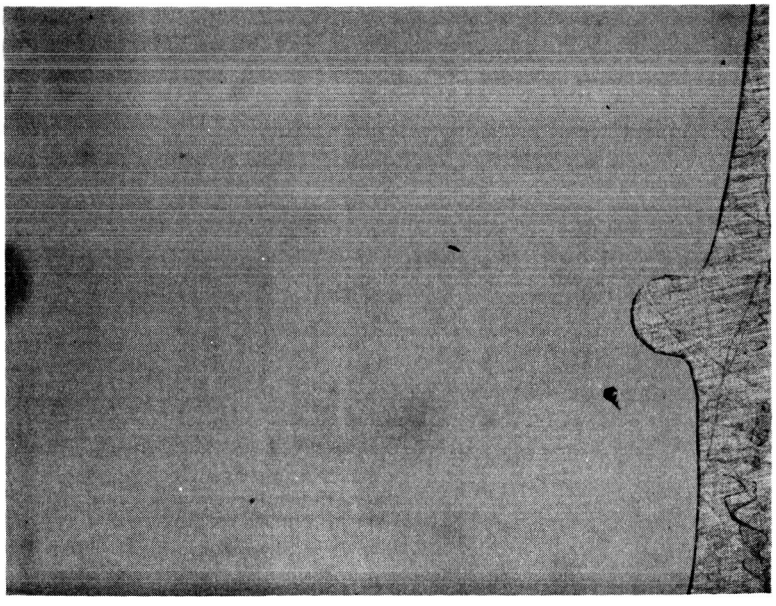
$$\ln (\text{yield}) = -NA \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (22)$$

where N is the number of imperfections/cm^2, and

A is the area of space change width of the collector-to-base junction.



a. 1000/cm^2



b. Less Than 5/cm^2

FIGURE 14 PINHOLE DENSITY IN SILICON DIOXIDE COATING ON WAFERS, AS OBTAINED BY THE CHLORINE ETCH TEST

A final diffusion yield was computed that compared quite well with the actual values.

Extreme care was exercised in cleaning the wafer surfaces, removing moisture from their surfaces, and in filtering KPR. This care resulted in a reduction of pinhole counts to approximately $100/cm^2$. However, a further reduction of pinholes was necessary. This was obtained by replacing the KPR with a mixture of KPR and KPL. An immediate reduction of pinholes was observed in the clorine etch test (see Figure 14b) when this new formulation was introduced into the standard process. Subsequently, many wafers were processed which were virtually free of imperfections.

The decrease in the incidence of pinholes in the photoresist film was attributed, in the final analysis, to the new formulation plus the application of a thicker film to the wafer surface. For a given whirling speed, the KPR-KPL formulation was approximately 75 percent thicker than that normally indicated with KPR. Although the use of this system resulted in a loss of definition, one-mil lines were easily obtained.

The usual photoresist problems associated with high relative humidity, such as poor adhesion and definition, were encountered during this program. In order to minimize these effects, a series of controlled atmosphere storage areas were constructed. The photoresist itself was stored in closed bottles in a dessicator. All coated wafers were dried in a container equipped with a continuously flowing

stream of filtered dry nitrogen. When wafers were not being processed, they were stored in similar containers. A 200°C wafer baking operation, just prior to coating, was also initiated in an attempt to keep the wafers dry.

3. The Overlay Structure

One of the important studies conducted during this program was the feasibility of placing isolated emitter sites in the base area and connecting them with emitter metallizing over the base metallizing, separated by an insulating layer. RCA feels strongly that this structure called "overlay" will produce the next family of high performance silicon transistors. This technique allows for:

a) A large decrease of unusable base and emitter area, thereby greatly increasing the emitter periphery collector–base area ratio and lowering the capacitance.

b) A substantial reduction of voltage drops in the emitter because the whole area of the device can be used to conduct emitter current.

c) Greater flexibility in designing transistors with secondary break protection because separate emitter sites are used.

A transistor, which incorporates the design illustrated in Figure 9, was used to study the effectiveness of this structure. The evaporation of silicon monoxide through a metal mask was the approach selected for fabricating the insulating layer. The major problems

encountered were voids in the film and poor adhesion in subsequent processing. The oxide was difficult to etch, resulting in a tedious metal mask alignment and evaporation cycle rather than a photoresist definition process. The evaporation source was a tantalum Drumheller type crucible that was set 10 inches below the aligned wafer. A movable shutter was placed between the work and the source, which also acted as the ion bombardment cathode plate. The work was the anode. Evaporations were performed at a final pressure of 5×10^{-6} mm of mercury. The evaporation rate was 1000 Å per minute, controlled by a voltmeter on the power supply and monitored by the rate of interference color changes.

The difficulty of fabricating films, that adhered to the substrate and were free of voids, was overcome by employing stringent substrate clean-up procedures and by increasing the film thickness. The thick films provided pinhole-free coatings combined with a sufficient quantity of silicon monoxide to coat the steep sides of the base aluminum contacts. For a 40,000 Å thick aluminum stripe, silicon monoxide layers 10,000 Å thick had to be evaporated to achieve complete insulation.

In order to eliminate scattering of silicon monoxide under the metal mask, a baffle plate was placed 1-1/2 inches above the source. In addition to accomplishing the task of improving definitions, this technique also improved adherence to the substrate.

The voids in the films, attributable to dust particles and mask defects, were eliminated by a double evaporation and by offsetting the mask.

Employing these techniques on only a few wafers resulted in a 50 percent yield of emitter-to-base insulation. The evaporated silicon monoxide had a dielectric strength of 10^6 volts per centimeter.

Although the insulation of the emitter from the base was accomplished on a fairly complex transistor structure, many other questions remained unanswered. The effects of the subsequent alloying mounting, bonding and environmental testing operations were unknown. Because of these unknown quantities and the fact that the required device parameters could be attained by utilizing the conventional, higher reliability planar passivated type structures, the "overlay" program was discontinued at this point in its development. However, it is felt that this unit can be made and is worthy of further study.

4. Metallizing

a. Surface Leakage

High reverse currents were observed in planar transistors on the collector-to-base, emitter-to-base and collector-to-emitter testing which followed the metallizing operation. This effect was most noticeable in the TA2379 pattern (see Figure 8) in which the metal extends over the oxide that covers the p-n junctions. However, the same type of degradation has been observed at various times in most planar units. The V-I characteristics of this degradation, as illustrated in Figure 15, are similar to those of a unipolar device and are indicative of a

"channel" type pinch-off.

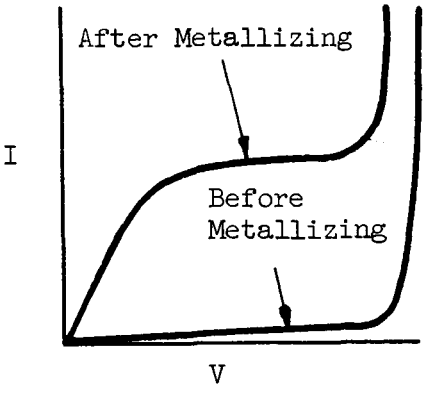


FIGURE 15 REVERSE BIASED JUNCTION DEGRADATION RESULTING FROM ALUMINUM METALLIZING

A series of experiments was performed in an attempt to isolate the cause of the degradation. The first experiments consisted of heat treatment studies on unmetallized, diffused wafers. Results of these experiments indicated that temperatures of 600 to 1000°C in either a nitrogen atmosphere or a vacuum or with a coating of photoresist on the wafer caused no reverse bias degradation when the units were cleaned prior to being subjected to heat treatments. However, the heat treatments did show that the presence of aluminum on the oxide, which covers the junctions, caused reverse bias degradation.

The most pertinent experiment performed consisted of evaporating aluminum over the surface of two diffused TA 2438 wafers, with their metal-contact areas open. One wafer was processed through the normal definition of the contact pattern.

This wafer showed no degradation of reverse current upon being heated. The second wafer, which was heat treated for three minutes at 530°C in a nitrogen atmosphere prior to aluminum pattern definition, showed severe I_{CBO} leakage (5 to 10 ma at 10 volts) and a "soft" breakdown voltage. The oxide was then etched from the second wafer, in 3000Å thick increments, and leakage current tests were performed on it after each cycle. As illustrated in Figure 16, very little decrease occurred in reverse current until more than one-half of the oxide was removed, then a rapid reduction occurred. Thus, results of this experiment indicated that the high reverse currents obtained after metallizing are caused by heat treating a transistor upon which aluminum is in contact with the oxide that covers the junctions. Furthermore, the results of this experiment indicate that the degradation mechanism causes a direct change in the passivating properties of the silicon dioxide layer. This effect is made on the interior rather than on the surface of the oxide.

In other experiments conducted in this area, the following results were obtained:

a) All metals did not cause the same reaction as aluminum.

b) Raising the base surface concentration of the transistor minimized degradation.

The results obtained from the experiments has led to the formation of a model which attempts to explain the occurrence of high

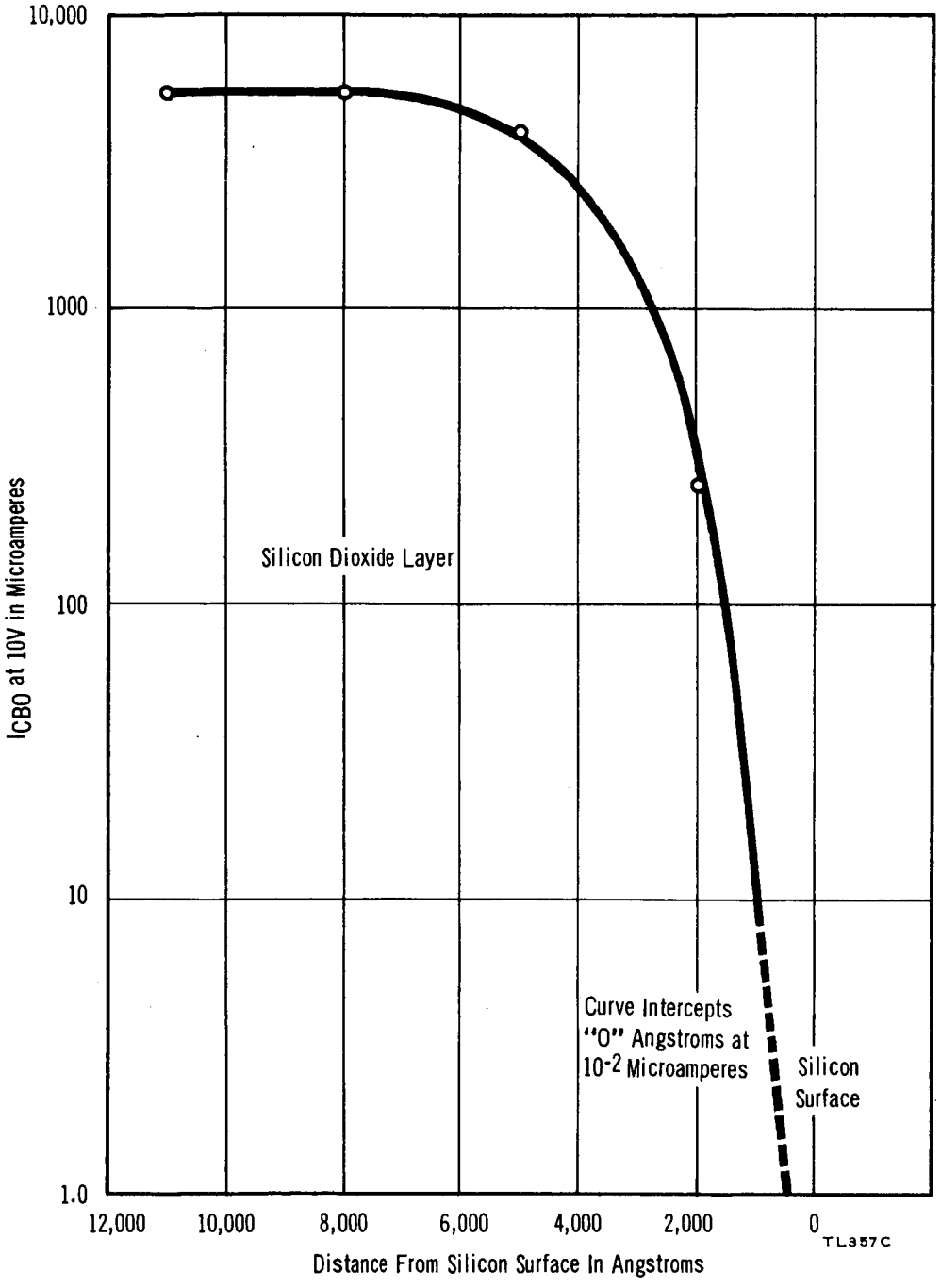


FIGURE 16 EFFECT OF REMOVING PASSIVATING OXIDE FROM A DEGRADED JUNCTION WITH CHANNEL TYPE V-I CHARACTERISTICS

reverse saturation currents resulting from aluminum contacting. The basic premise of the model is that the leakage is caused by a channel on the surface of the base, under the oxide, which pinches off at low voltages. The channel is not present after diffusion, although a condition exists that makes the formation of a channel possible; a low base surface concentration ($\sim 10^{18}$ atoms/cc p-type concentration).

The channel is formed by an inversion layer on the base which converts that surface to an n-type layer. The n-type layer forms a non-linear (i.e. current dependent) resistor which shunts the collector-to-base and emitter-to-base junctions and then pinches off due to the voltage built up by the current flowing through the channel.

The inversion layers are apparently induced in the surface by the heat treatment of the wafer, with aluminum over the oxide covered junctions. It is suspected that the aluminun diffuses into the silicon dioxide structure and causes cationic slow states to form in the oxide. As shown by Atalla, the presence of positively charged states, away from the silicon surface, can induce an inversion layer to form on p-type material by the electrostatic attraction of electrons[11]. Although there is no data in the literature to support the theory that aluminum diffuses in the silicon dioxide, it is felt that this is still a probable explanation for the mechanism.

The metallizing fingers on the TA2379 extend from the contact areas of the four bases on the oxide layer, over the junctions, to the bonding areas. Because of this design, the reverse characteristics of the unit deteriorate when it is heat treated above 400°C. Experimental units were made in which p^+ diffusions surounded the emitter sites in the base region. These units met with some success in that their I_{CBO} values were as low as 50 nanoamperes after bonding. However, many processing problems were encountered with this approach.

Because of these problems, combined with the fact that the diffusion yields were not greatly improved, the TA2379 unit, which incorporates aluminum metal extending over junctions on the oxide, was replaced by the more conventional TA2438 unit.

Occasional degradation of TA2438 units was experienced during evaporation. Indirect measurements made on the evaporated wafers indicated that the surfaces of the wafers attained temperatures above 500°C during an evaporation of 8 to 10μ of aluminum. Wafers covered with aluminum will have deteriorated junctions when exposed for a short period to a temperature of 500°C. Therefore, it became apparent that the evaporation power had to be kept at a minimum and a good heat dissipation path had to be provided for the wafer during evaporation. Units were processed through metal evaporation with these requirements incorporated in the conditions. The resultant units revealed I_{CBO}, I_{CEO} values, at 50 volts, as low as two nanoamperes.

The median value, as reflected in Figure 17, was 25 nanoamperes.

b. Contact Resistance

Good ohmic contact between the aluminum contact metal and the emitter and base portions of the silicon is an important factor in determining high current capabilities of the transistor pellet. The simplest technique for obtaining low contact resistance is to form an aluminum-silicon eutectic alloy by heating the elements above 570°C. Unfortunately, this simple technique can destroy the junctions. The problems created by aluminum penetrating through the shallow junctions, caused by uneven alloying, are always present. Bonding to an aluminum-silicon eutectic creates another problem. These and other considerations make the formation of a low resistance contact, at lower temperatures, a distinct processing advantage.

Previous ohmic-contact work at RCA has revealed that, when wafers are heated to temperatures of 50°C below the aluminum-silicon eutectic temperature, a distinct drop in contact resistance occurs. When the aluminum was stripped from the contact areas, a disturbance of the silicon surface could be noted. Further work in this area under this contract led to the conclusion that this effect is related to the surface concentration of the diffusants. Generally, the emitter areas show the largest degree of etch pits, triangles, etc. The base does not show quite the same degree of distrubance, while the undiffused

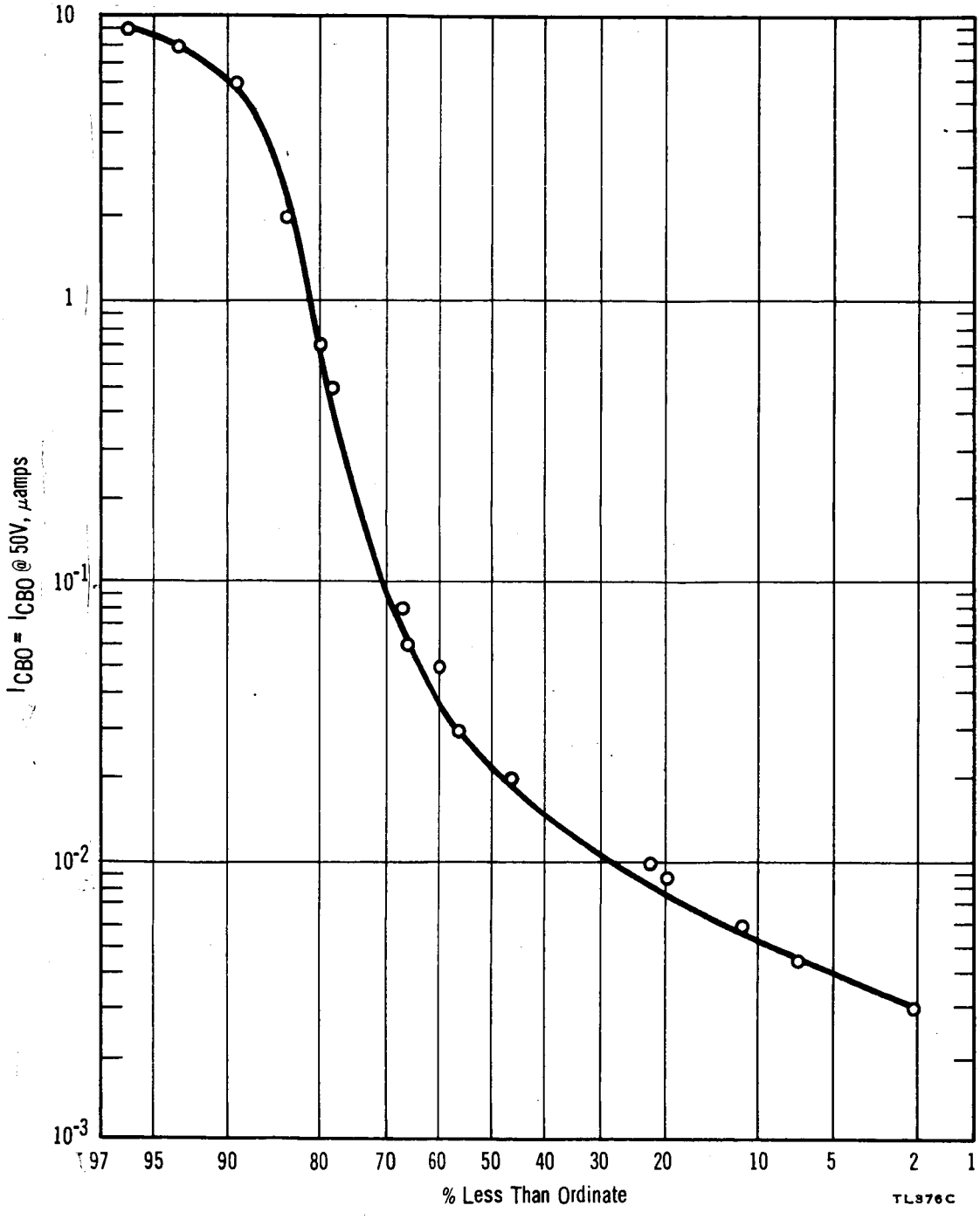


FIGURE 17 LOGARITHMIC DISTRIBUTION OF I_{CBO} @ 50V

silicon collector, exposed in scribe lines, shows very little if any change in the surface.

The contact resistance as measured by V_{EB}(forward) or V_{CE}(SAT.) is not lowered further when the device is heat treated above 530°C. This evidence seems to indicate that a form of micro-alloying or diffusion occurs on the surface of silicon that has been severely strained by oxidations and diffusions. This "surface alloying" phenomenon can occur from the heat of a high power aluminum evaporation. However, when this happens it is very often accompanied by junction degradation. Therefore, the standard procedure has been to maintain a low temperature on the wafer during evaporation, followed by a heat treatment at 530°C for 3 minutes, after the metallizing pattern has been defined.

B. PACKAGING

1. Isolated Collector

The isolated collector package was designed to create a package capable of high power dissipation that could be electrically isolated from heat sinks. Collector isolation was previously achieved through the use of external insulators made of materials such as mica. However, this method of isolation seriously reduced the thermal dissipation of the unit and, therefore, its current handling capacity. In addition, its reliability was questionable.

Prior efforts directed toward the production of isolated collector packages for power transistors have revealed that beryllium oxide is the best package insulating material. The thermal conductivity of this material is 2.1 watts/cm-°C, the lowest known value for a ceramic. In addition to this advantage, beryllium oxide has fair mechanical strength and can be metallized to form solderable contacts. Other properties of beryllium oxide and of aluminum oxide, another common insulating material, are compared in Table VII.

The major disadvantage of beryllium oxide, when used as an isolated collector insulating material, is that its coefficient of thermal expansion is less than that of the copper base.

In the initial approach toward the development of an effective isolated collector package, a molybdenum tab was placed between the copper base and the beryllia pellet. The purpose of the tab was to act as a buffer against the stresses caused by cooling. High temperature brazes were used to solder the molybdenum tab to the copper base and the beryllia pellet to the molybdenum tab. This innovation was not successul. In addition, the use of the tab resulted in a considerable increase in thermal resistance.

The final approach involved the use of a low temperature soft solder, between the beryllium oxide and the molybdenum tab, as a stress relief during temperature cycling. Lead was chosen as the soldering material. Initial results of this approach were successful, i.e., cracking of the pellet was eliminated. The molybdenum tab was then

TABLE VII

COMPARISON OF BERYLLIUM OXIDE AND ALUMINUM OXIDE PROPERTIES

Property	Beryllium Oxide	Aluminum Oxide
Thermal		
Maximum Temperature	1316°C	1510°C
Expansion Coefficient at 25 to 100°C	3.45×10^{-6}	5.19×10^{-6}
25 to 400°C	6.62×10^{-6}	6.76×10^{-6}
25 to 700°C	7.78×10^{-6}	7.41×10^{-6}
Thermal Conductivity	0.323 cal/sec-cm-°C	0.40 cal/sec-cm-°C
Mechanical		
Compressive Strength	200,000 lbs/in.^{2}	386,000 lbs/in.^{2}
Flexural Strength	27,000 lbs/in.^{2}	49,000 lbs/in.^{2}
Hardness	8 mohs	9 mohs
Electrical		
Dielectric Strength	220 volts/mil	234 volts/mil
Resistivity at 500°C	370×10^6 ohms	108×10^6 ohms
at 700°C	80×10^6 ohms	18×10^6 ohms

eliminated in an attempt to decrease thermal resistance. This approach was found to be feasible and was incorporated into the fabrication process.

2. Pellet Mounting

The two major problems encountered in mounting silicon pellets to the case were inadequate wetting of the interfaces and the degradation of characteristics. These two modes of failure are interrelated.

A gold-silicon alloy is used to mount pellets on the beryllia insulation. This alloy prevents dissolution of excess silicon that could penetrate to the collector junction. The agitation and pressure used in the mounting system facilitates wetting of the solder to the silicon, by breaking oxides which form on the solder. A forming gas atmosphere was initially used to minimize oxidation during this process. Because heating the transistor in a hydrogen atmosphere degraded its reverse characteristics, a nitrogen ambient was substituted in the mounting furnace. Before the pellets were heated in the furnace, they were cleaned in acetone to remove dust particles or other contaminants that could lead to deteriorated characteristics.

During the mounting operation, pellets were periodically checked for complete wetting by lifting them off the beryllia while the solder was still molten. Voids in the solder-silicon interface resulted in an extremely poor local, thermal-heat path. This condition caused

local heating at the junctions and, thereby, seriously limited the power handling capabilities of the unit. Thermal resistance measurements made on units, which had voids in their solder-silicon interfaces, have shown values as high as 4°C/watt. This happened on rare occasions, however, as the thermal resistance of the units formed a tight distribution of 0.8 to 1.5°C/W. (See Figure 1.)

C. REDUCTION OF SWITCHING TIMES

The relationship of storage time to device geometry is given by

$$\tau_s = \frac{W^2}{2D_n} + \frac{a^2}{2D_p} \ln\left[\frac{2}{\frac{\beta_F}{\beta_n} + 1}\right]$$

where $\frac{W^2}{2D_n} = \frac{\tau}{\beta_n}$.

Therefore, the three variables that influence τ_s most are collector thickness (a), current gain (β_n) and minority carrier lifetime (τ). Current gain should be kept at a minimum because the term ln (β_n) has the greatest effect on switching time. The plot of current gain versus τ_s, as illustrated in Figure 18, shows that this dependence does exist. The scatter of points on the curve is due, primarily, to variations in thickness (a) of the undiffused collector region. This region should be kept as narrow as possible.

The minority carrier lifetime should also be kept at a minimum. However, the reduction of this variable is difficult to accomplish. Gold diffusions have been used for this purpose, however, this approach creates

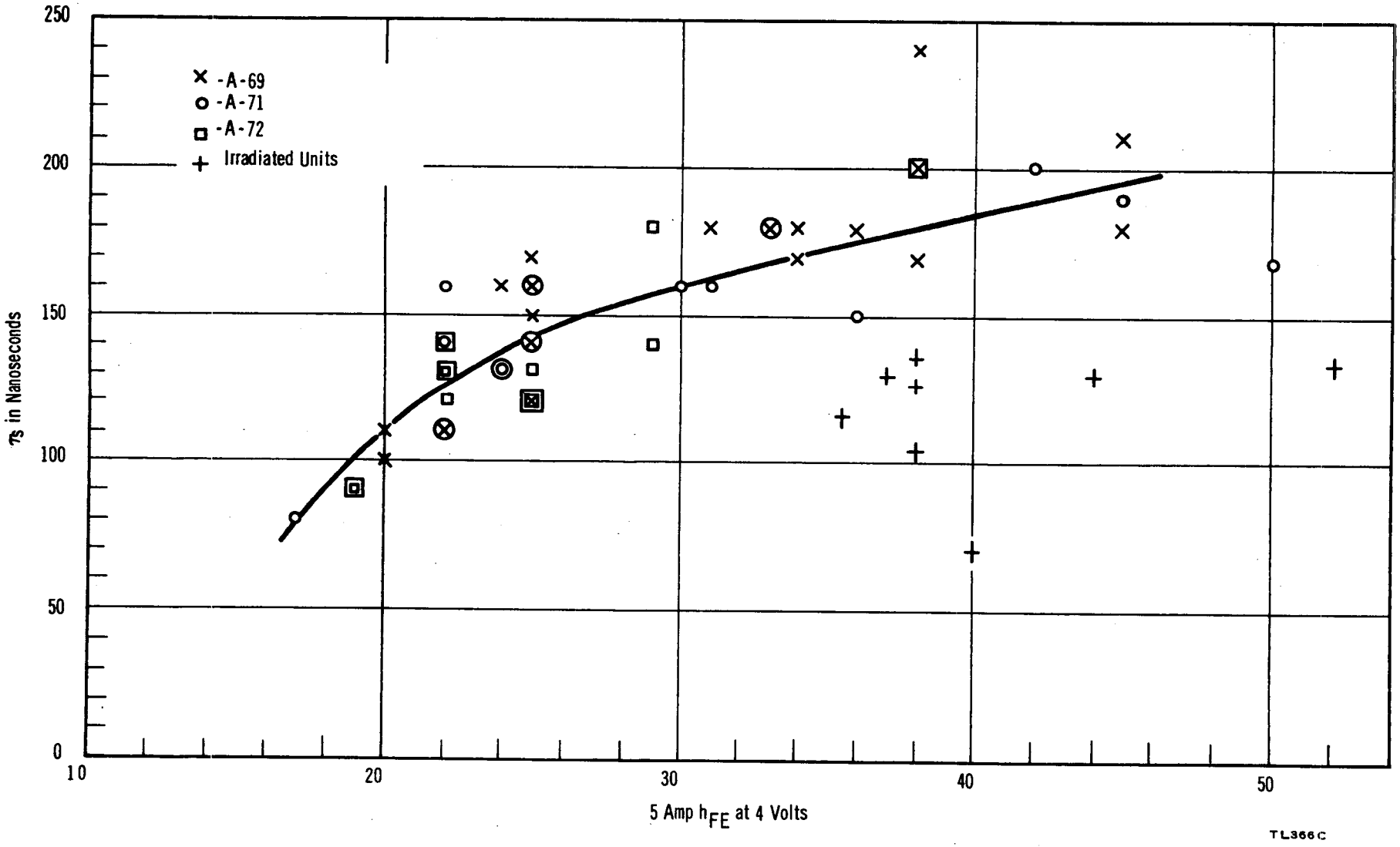


FIGURE 18 h_{FE} VERSUS STORAGE TIME, τ_s

processing problems, such as junction degradation, and results in high saturation voltages.

Another method used to reduce minority carrier lifetime consists of subjecting the devices to electron beam radiation. This method was used on several mounted, but unsealed transistors. The units were irradiated with one Mev, in a Van de Graff generator, at two different flux densities. A substantial reduction in the storage time of the devices, as well as a small reduction in their current gain, was achieved. Figure 18 shows that the irradiated units have shorter storage times for a given h_{FE} value than units that were not irradiated. Table VIII presents a more detailed description of the effect of electron beam radiation on device performance. Environmental studies would have to be made on devices, subjected to this approach for reducing minority carrier lifetime, to determine their stability.

TABLE VIII

CHARACTERISTICS OF ELECTRON RADIATED DEVICES

Condition	2A 20A	2A 20A	*	20A 4V	10A 4V	5A 4V	1A 4V	2A 2.5V	10V	10V	50μA	50μA	50μA	50mA	50mA
Parameter	τ_S ns	τ_F ns	Σ_T sec	β_N	β_N	β_N	β_N	β_I	I_{CBO} (mA)	I_{CEO} (mA)	V_{CBO} (Volts)	V_{CEO} (Volts)	V_{EBO} (Volts)	$V_{CEO(SUS)}$ (Volts)	V_{CBO} (Volts)
A69-8	220	50		57	59	62.5		3.3	$.38\times10^{-3}$	$.35\times10^{-3}$	124	93	9.5	65	140
	170	30	50	46.5	50	62.5		0.95	$.42\times10^{-3}$	$.42\times10^{-3}$	123	95	9.5	61	138
	130	25	100	40	41.5	45.5		0.53			122	94	9.6	59	135
A69-14	230	70		50	54	57.5		3.85	$.19\times10^{-2}$	$.34\times10^{-1}$	96	24	6.6	50	136
	150	30	50	40	38.5	53		1.0	$.16\times10^{-2}$	$.14\times10^{-1}$	102	50	6.6	61	132
	125	25	100	36	38.5	38.5		0.51			106	57	9.0	59	130
A69-9	220	50		57	64	62.5		3.64	$.4\times10^{-3}$	$.4\times10^{-3}$	127	122	10.7	60	140
	130	30	100	59	44.5	45.5		0.47	$.14\times10^{-3}$	$.14\times10^{-3}$	127	122	10.5	61	140
	100	25	200	36	38.5	38.5		0.21			126	120	10.5	60	137
A69-48	280	40		50	57	57.5		2.74	$.68\times10^{-2}$	$.67\times10^{-2}$	120	120	0.5	90	140
	220	40	100	44.5	47.5	47.5		1.25	$.72\times10^{-3}$	$.76\times10^{-3}$	128	128	1.0	85	144
	135	25	100	33	38.5	38.5		0.36			123	84	8.7	83	140
A69-31	200	50		77	93	76	55	3.1			115	115	2.3	57	132
	130	30	140	50	51	52	43	0.4			116	116	8.8	56	134
A69-16	220	70		57	65	66	63	3.7			99	99	0.3	62	135
	70	30	200	28	38.5	40	40	0.16			100	100	0.9	60	134
A69-46	270	50		61	67	66	63	3.15			118	116	4.8	73	140
	115	25	200	33	36	35.5	32	0.25			120	120	5.0	85	140
A69-45	270	80		57	67	67	63	3.15			124	124	9.3	76	140
	130	30	200	33	37	37	32	0.25			124	124	9.3	87	140

* Σ_T represents the total exposure time compensated for angle of incidence if necessary

VI. TESTING RESULTS

A. INTRODUCTION

Testing the transistor, in all stages of its development, is one of the most important operations performed in fulfilling a development contract. Testing is a measure of progress, an experimental tool, and the means by which process control is enforced. During the initial stages of development, testing is an aid to establishing a process capable of producing the required unit. Having established this process, emphasis is placed on the evaluation and analysis of the devices produced by this process. The information obtained is then utilized to optimize the process in terms of producing devices with best characteristics.

For discussion purposes, testing is divided into two major categories in this report. The first section explains the system of in-process inspections and tests performed during the fabrication stage. The second section evaluates the characteristics of the submitted devices. A complete report which details the inspection steps incorporated in the normal processing procedure was forwarded to NASA in March 1963.

B. PROCESS TESTING

The physical and electrical tests performed on devices during their fabrication serves two distinct purposes. In the initial development of the process it is the means for evaluating process feasibility. Once the process is established, "in-process" inspection is used to monitor the device to insure product reliability and reproducibility.

It also serves as an initial evaluation of changes made in the "standard process", as a result of feedback information. The testing described in this section is indicative of the process control tests that have been established for this transistor.

The physical or non-electrical tests performed have an important role in controlling the process. These tests were detailed in Section IV of this report, therefore, they will not be described here. This section will restrict itself to the in-process electrical evaluation of the transistor. The last three diffusion runs processed exhibited the best yields and appeared to be quite reproducible.

The first electrical test performed is a reverse bias I-V test on the base diode using a Tektronix (type 575) curve tracer. From the characteristic of this curve, an important initial evaluation of device yield is obtained. The effects of factors such as bulk impurities, effective boron concentration and starting material homogeneity can be observed from a knowledgable examination of this parameter.

A more elaborate electrical test of junction characteristics is performed, following the emitter diffusion and the definition of contact areas. The collector-to-emitter, collector-to-base and emitter-to-base junctions can be observed in the reverse bias condition, and a reliable dc device yield can be obtained. The testing at this point is restricted to low current levels because of the contact resistance of the silicon surface. The deterioration

of junctions due to emitter-to-collector n-type "pipes", high leakage currents and low breakdown voltages, resulting from junction periphery effects, are obtained at this stage. Occassionally, microplasma emissions at breakdown are examined, in order to further determine the mechanism of junction failure. The information obtained from the devices which have "good" characteristics is a measure of the diffusion control with regard to impurity concentrations and junction gradients.

After initial contacts have been formed on the device, a more rigorous quantitative test is made at the reverse-bias, low-current level condition. The tests made at this point serve as a control on the metallizing operation. (This operation has caused degradation of junctions). High reverse current and soft breakdowns that are current sensitive are two conditions that are specifically checked. A forward bias emitter-to-base junction test is also performed to determine the surface contact resistance of the emitter and base metallizing.

After pelletizing the wafer and mounting the individual units, high power tests can be performed. The mounting operation provides both the low resistance collector contact and a heat sink for heat dissipation. However, the current handling ability of the device is governed by probe contact resistance, thereby limiting the high current testing to a one-ampere h_{FE} measurement. Reverse bias parameters are reinspected as a monitor on deterioration which results from processing the device through the mounting furnace.

Once the units are bonded, all of the electrical testing can be made and the results compared to the contract requirements. The results obtained from these tests determine what units are to be sealed. Furthermore, the measurements of high current gain, saturation resistance and switching times furnish information not previously attainable, i.e., information relative to base width and collector region thickness. This information is then fed back into the earlier stages of the operation to guide further device fabrication. The testing methods and equipment used are listed in Table IX.

The high power and dynamic tests performed at this time are h_{FE} at 10 and 20 amperes, saturation voltage at 20 amperes with an input of 2 amperes, switching time measurements and thermal resistance. Both saturation resistance and high current gain are measured with a high current adaptor, Tektronix type 175, in conjunction with a Tektronix, type 575, curve tracer (see Figure 19). The curve tracer is equipped with separate current and voltage leads to eliminate voltage drops in lead wires. The switching time measurements are performed with the specially designed circuit shown in Figure 20, which incorporates a Tektronix 545A oscilloscope. The devices were turned off from a condition of 20 amperes collector current at +2 ampere base drive to a -2 ampere base current.

Thermal resistance was tested on every unit as a check on the mounting technique and the beryllium oxide metallizing. The

TABLE IX

SPECIFICATIONS AND TESTING METHOD

Specification	Operating Point	Testing Method
h_{FE} greater than 10	I_C = 20A, V_{CE} = 1.5V	Tektronix type 575 curve tracer with a type 175 high current adapter. Separate current and voltage leads used.
$V_{CE(sat)}$ less than 1.5V	I_C = 20A, I_B = 2A	
$V_{BE(sat)}$ less than 3.5V	I_C = 20A, I_B = 2A	
I_{CBV} less than 30ma	T = 200°C, V_{EB} = 1.5V, V_{CE} = 125V	Oven and Tektronix type 575 curve tracer
I_{EBO} less than 25ma	T = 200°C, V_{EBO} = 10V	
τ_{off} less than 250 nanosec.	I_C = 20A, I_{BI} = I_{B2} = 2A	Special circuit and Tektronix 545 oscilloscope.
τ_{on} less than 250 nanosec.	I_C = 20A, I_{BI} = I_{B2} = 2A	
θ_{jc} less than 1.2°C/watt	Variable I_B = 1.5 amps ΔT = 20 to 25°C	Tektronix 541 oscilloscope and special circuit using V_{BE} as the temperature sensitive parameter.

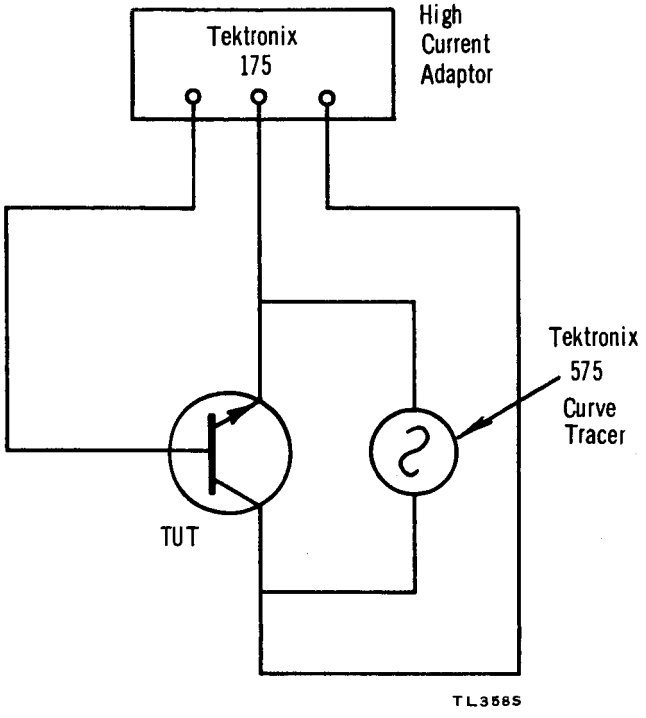


FIGURE 19 BLOCK DIAGRAM OF HIGH CURRENT TEST EQUIPMENT

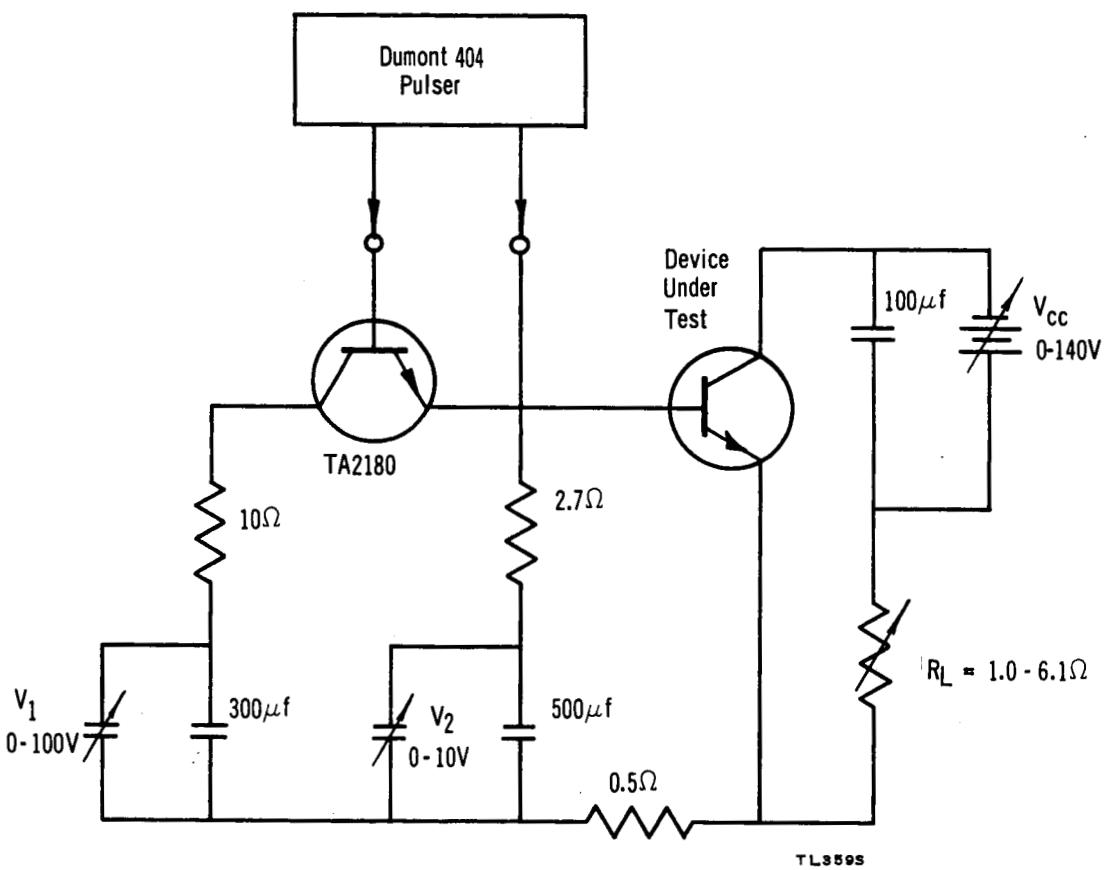


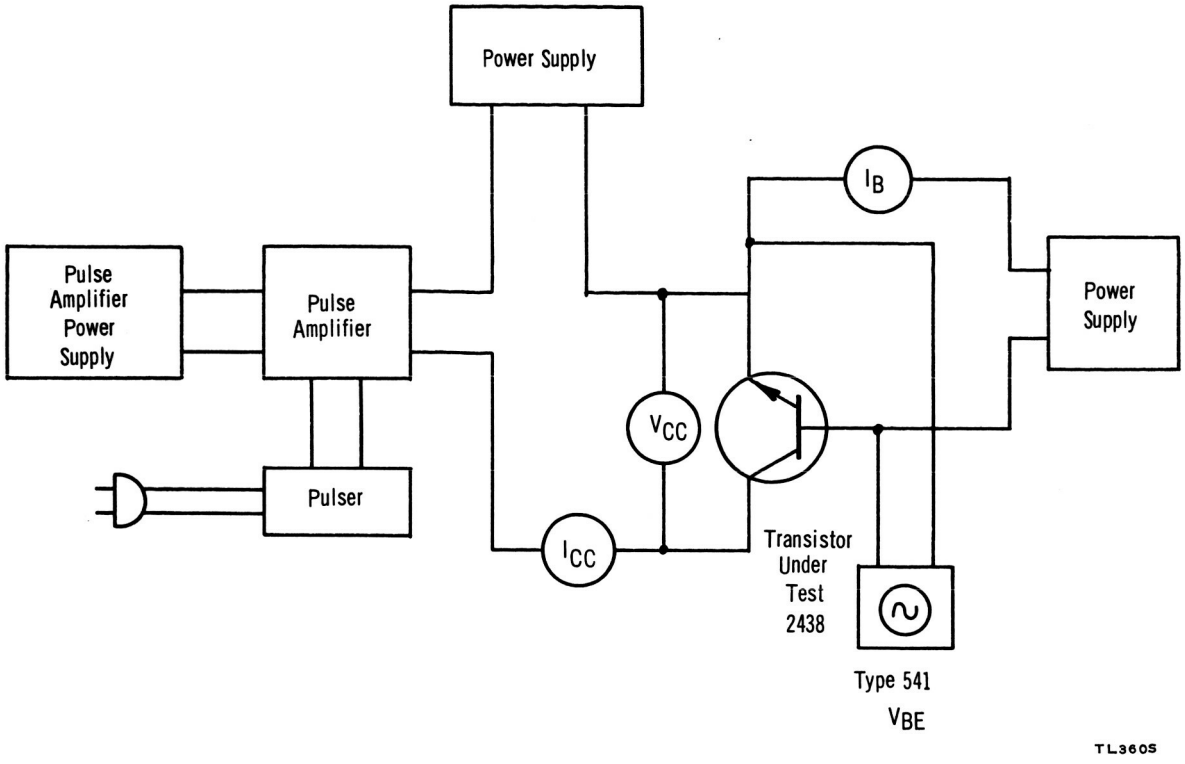
FIGURE 20 TEST CIRCUIT FOR TURN OFF TIME

measurements were made by monitoring the change in V_{BE} with increasing device temperature resulting from power dissipation. The measurement is made on Tektronix (type 541) oscilloscope equipped with a Type Z plug-in unit for sensitive voltage measurement. A diagram of the test circuit is shown in Figure 21. All measurements were made at a collector current of approximately 1.5 amperes and a temperature differential of approximately 20°C. The conditions were arrived at in a manner such that the measurement was not influenced by local thermal effects due to second breakdown. This was accomplished by keeping the collector voltage in the 10 to 15 volt range, which is generally free of this condition.

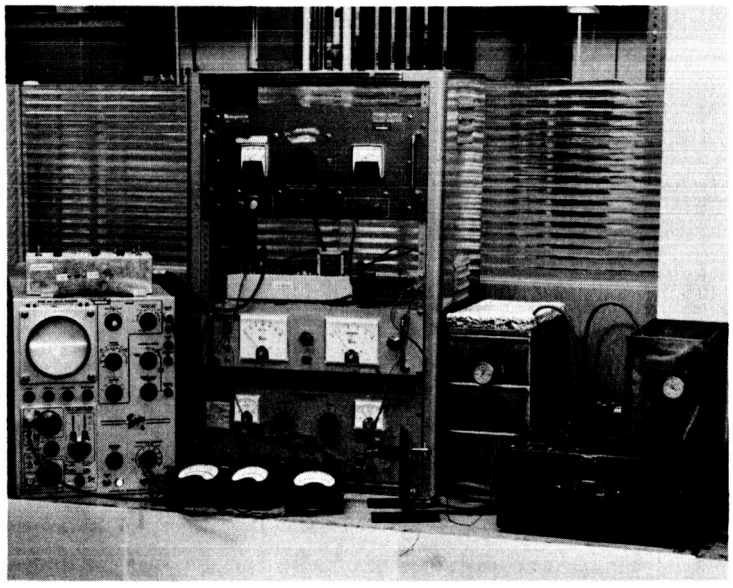
After the units have been sealed, they are retested. The units which were shipped to the contracting agency were subjected to tests such as, collector capacitance, V_{BE}, and high temperature reverse bias. Comparison of the pre-sealing results to post-sealing data showed only one shift in value. The saturation voltage at 20 amperes increased from 0.1 to 0.2 volt because of voltage drops in the shell-to-post connection. The final units were then selected for shipment. The electrical characteristics of these final units are shown in Table X.

C. ENVIRONMENTAL TESTING

After a sample group of units were subjected to a variety of environmental tests, their mechanical and electrical stability was measured. Prior to the selection of the sample group, all units were subjected



a. Test Circuit



b. Test Set

FIGURE 21 THERMAL RESISTANCE TEST CIRCUIT AND TEST SET

TABLE X

ELECTRICAL CHARACTERISTICS OF FINAL UNITS

PARAMETER	I_{CBO}	I_{CEO}	I_{CEX} V_{EB}=1.5	I_{EBO}	BV_{CBO}	BV_{CES}	$VCE_{(SAT)}$	$VBE_{(SAT)}$	h_{FE}	h_{FE}	h_{FE}	t_d+t_r	t_s $I_{B_1}=I_{B_2}$ = 2A	t_s+t_f	C_{ob}	θ_{J-C}
MEASUREMENT			200°C	200°C			I_B=2A	I_B=2A	V_{CE}=4V	V_{CE}=4V	V_{CE}=4V		I_C = 20A			
POINT	50V	50V	100V	8V	100ua	100ua	I_C=20A	I_C=20A	I_C=1A	I_C=5A	I_C=20A		V_{CE} = 28V		10V	I_B=1.5A
UNITS	ua	ua	ma	ma	Volt	Volt	Volt	Volt				Nsec	Nsec	Nsec	pf	C°/Watt
DEVICE																
A66-8	.055	.055	.07	.08	107	107	0.95	1.55	31	36	40	140	180	250	380	0.8
A66-26	.3	.3	.10	2.0	120	120	1.20	1.50	45	45	40	140	180	260	378	1.36
A66-38	.6	.6	.09	.1	110	110	1.10	1.40	36	38	37	130	170	200	372	1.31
A67-19	.7	.7	.07	4.0	115	115	1.2	1.9	32	34	33	130	170	250	368	.67
A67-22	.02	.02	.16	.11	120	120	1.1	1.3	31	33	33	130	180	240	362	1.21
A68-14	.34	.34	.19	2.5	105	105	.65	1.3	29	31	33	140	180	250	426	1.05
A69-2*	.02	.02	.17	.5	115	110	.73	1.3	25	25	25	130	140	220	451	1.04
A69-4	.012	.012	.06	.25	115	115	.7	1.3	24	24	24	140	160	220	407	.85
A69-11	.01	.01	.08	.14	115	110	.75	1.3	25	25	25	130	150	200	449	1.95
A69-13	.011	.014	.06	1.5	105	105	.62	1.3	40	38	33	130	200	260	432	1.05
A69-27	15.	15.	.17	1.6	110	110	.6	1.3	32	34	36	140	180	220	398	1.44
A69-28	10.	38.0	.22	0.4	115	115	.78	1.3	24	25	22	150	120	180	425	1.81
A69-35	7.5	7.5	.11	1.6	110	110	.8	1.3	20	20	20	150	100	150	387	1.05

TABLE X (Cont.)

PARAMETER	I_{CBO}	I_{CEO}	I_{CEX} V_{EB}=1.5	I_{EBO}	BV_{CBO}	BV_{CES}	$VCE_{(SAT)}$	$VBE_{(SAT)}$	h_{FE}	h_{FE}	h_{FE}	t_d+t_r	t_s $I_{B_1}=I_{B_2}$ = 2A	t_s+t_f	C_{ob}	θ_{J-C}
MEASUREMENT			200°C	200°C			I_B=2A	I_B=2A	V_{CE}=4V	V_{CE}=4V	V_{CE}=4V		I_C = 20A			
POINT	50V	50V	100V	8V	100ua	100ua	I_C=20A	I_C=20A	I_C=1A	I_C=5A	I_C=20A		V_{CE} = 28V		10V	I_B=1.5A
UNITS	ua	ua	ma	ma	Volt	Volt	Volt	Volt				Nsec	Nsec	Nsec	pf	c°/Watt
DEVICE																
A69-37	8	8.5	.06	8.0	100	100	.62	1.3	27	25	25	140	170	250	448	1.21
A69-41	.003	.003	.03	0.20	112	112	.82	1.45	24	25	25	150	160	200	383	1.26
A69-42	.004	.004	.045	.17	105	105	.65	1.3	37	38	33	140	240	280	490	1.01
A69-50	5.7	5.7	.12	6.5	105	105	1.2	1.3	44	45	45	160	210	250	387	0.92
A69-53	.02	.02	.055	0.9	102	102	.68	1.3	20	20	20	140	110	170	472	1.13
A71-2	.22	.22	.15	.25	195	105	1.0	1.5	22	24	24	150	130	190	377	1.01
A71-6	.4	.4	.15	6.5	115	115	1.20	1.45	29	31	27	130	160	210	384	1.25
A71-7	.016	.016	.12	.2	110	110	.85	1.4	26	25	24	130	170	210	393	1.24
A71-8	.011	.011	.13	5.5	115	115	1.0	1.5	30	30	28	130	160	190	371	1.15
A71-10	.07	.07	.11	.12	105	105	.95	1.40	24	25	25	130	160	190	396	1.15
A71-11	1.0	1.0	.11	.8	103	100	1.1	1.5	14	17	16	160	80	150	386	1.09
A71-22	4.	4.	.08	.6	105	105	0.65	1.3	21	22	22	140	140	200	432	1.07
A71-23	.4	.4	.085	.25	105	100	0.65	1.3	37	42	33	140	200	250	472	.98
A71-24 *	6.0	6.0	.25	4.0	105	105	0.82	1.35	32	36	33	130	150	180	380	1.11
A71-28	.002	.002	.065	7.0	110	110	1.5	1.4	21	21	20	180	140	200	369	1.13
A71-31	.04	.04	.045	8.0	100	100	1.0	1.3	21	22	20	170	160	200	351	1.37

TABLE X (Cont.)

PARAMETER	I_{CBO}	I_{CEO}	I_{CEX} V_{EB}=1.5	I_{EBO}	BV_{CBO}	BV_{CCES}	$V_{CE(SAT)}$	$V_{BE(SAT)}$	h_{FE}	h_{FE}	h_{FE}	t_d+t_r t_s t_s+t_f	C_{ob}	θ_{J-C}
MEASUREMENT POINT	50V	50V	200°C 100V	200°C 8V	100ua	100us	I_B=2A I_C=20A	I_B=2A I_C=20A	V_{CE}=4V I_C=1A	V_{CE}=4V I_C=5A	V_{CE}=4V I_C=20A	I_{B_1} = I_{B_2} = 2A I_C = 20A V_{CE} = 28V	10V	I_B=1.5A
UNITS	ua	ua	ma	ma	Volt	Volt	Volt	Volt				Nsec Nsec Nsec	pf	C°/Watt
DEVICE														
A71-32	.007	.007	.080	1.5	115	115	0.89	1.35	33	33	22	140 180 240	379	1.15
A71-39	.005	.005	.075	0.35	105	105	1.25	1.6	46	45	40	170 190 270	371	1.29
A71-41	.02	.02	.17	0.3	100	100	1.2	1.4	24	24	21	160 130 200	335	1.18
A71-44	.012	.012	.14	.8	100	100	1.3	1.5	26	56	45	170 170 250	368	1.13
A72-14*	.009	.01	.18	1.5	100	100	.95	1.35	21	22	20	140 130 180	429	1.35
A72-19	.005	.005	.08	8.0	105	105	.7	1.3	22	25	22	140 120 170	440	1.53
A72-20	.026	.026	.22	6.5	100	100	.85	1.4	20	22	22	140 120 180	476	1.25
A72-22	.007	.008	.10	5.0	110	110	.9	1.4	27	29	29	130 140 200	384	1.73
A72-26	.008	.009	.12	0.7	110	110	.85	1.4	18	19	20	140 90 150	419	1.11
A72-28	.05	.05	.07	.4	115	115	.78	1.3	22	22	22	140 130 160	407	.99
A72-29	.008	.008	.13	.8	110	110	.85	1.35	18	19	18	140 90 150	430	.94
A72-40	.018	.018	.25	.3	100	100	.90	1.3	31	38	33	130 200 250	386	1.25
A72-46	.043	.043	.40	6.8	102	102	.79	1.4	23	25	22	150 120 180	432	1.19
A72-47	.010	.010	.20	.8	110	110	1.10	1.44	27	29	29	170 180 240	398	1.60
A72-61	.016	.016	.4	.37	105	105	.90	1.35	26	25	25	160 130 190	432	1.31
A72-63*	.013	.014	.3	9.5	105	105	.80	1.35	24	22	22	160 140 190	425	1.05

* PACKAGE NON-HERMETIC

to a hermetic seal test. Helium leak apparatus was used for this test. The results of the test revealed that the first units sealed exhibited approximately 15 percent non-hermetic seals. Improvements in processing, combined with more rigorous inspection, reduced this percentage appreciably in subsequent units. Of the last 30 sealed units tested, only one was non-hermetic.

An eight-unit sample was subjected to the mechanical and environmental tests in the following sequence:

a) 20g vibration at 100 to 2000 cps for 4 minutes in each plane,

b) 500g shock, 5 blows in each of 4 planes, and

c) 10,000g centrifuge (3 planes, 2 waves).

The devices passed all of the shock and vibrations tests, from both a mechanical and an electrical standpoint. There were two failures, however, in the centrifuge test. One failure was caused by a collector bond pulling away from the beryllia metallizing. The length of collector wire connecting the post to the beryllia surface was shortened on subsequent units, thereby reducing the stress on the joints. The other failure was caused by a base bond opening at the thermal-compression bond. A new construction, which shortens the length of the bonding wires, was incorporated into the process (see Figure 11a). Larger device samples should be processed through these tests to obtain more conclusive information. However, it should be noted that the final units were constructed in a much more rugged manner than the sample units tested.

Another major area of environmental inspection is one in which units are subjected to different temperatures. Six units were subjected to the -65°C to 200°C temperature cycling test. No failures were detected, however, in two units collector base breakdowns were increased by 10 volts (90 to 100 volts).

Shelf Life tests at 200°C were performed on several small samples. The initial tests were performed in order to obtain information on different pre-sealing surface treatements. Units subjected to a liquid cleaning and a silane process were compared to units cleaned by a filtered stream of dry air. Though the samples tested were not large enough to produce conclusive data, the trends indicated that the air blasted units were at least as stable as the silane units.

A sample of five units was placed on shelf life at 200°C. Data was taken after 230 hours which indicated that some changes occurred in the properties of the units. On some units the 200°C bake produced good effects. Two of the units showed a slight increase in breakdown and a decrease in I_{CBO}. In one case the decrease was from 7×10^{-7} amperes to 2×10^{-8} amperes. A decrease in both switching time and high current h_{FE} was also noted. Two of the units exhibited some instabilities of I_{CBO}, although both units were still below one microampere at 50 volts. In order to fully explore this area, a larger sampling of units, having a broad range of properties should be processed. Neither time nor units were available to undertake this type of program under this contract.

D. FINAL RESULTS

This section analyzes the electrical characteristics of the final TA2438 transistors produced under this contract. Data which reflect the status of the units in diffusion run sequence is presented in Table X. A comparison of the tested results to those computed in Section III should prove interesting.

Direct-current, reverse-bias conditions were tested first. Room temperature leakage currents were tested at 50 volts using a Kelthley 610A electrometer. A distribution of current levels obtained is shown in Figure 17. The median value is at 25 nanoamperes. Some units reflect currents as low as 2 to 5 nanoamperes, while others reflect currents as high as 10 milliamperes. This indicates that, although problems associated with surface leakage currents have been solved, there is still work to be done in this area. One of the achievements of this program was obtaining identical values of reverse current between the collector-to-base and collector-to-emitter connections. This was accomplished by designing the unit such that the base metal completely surrounded the emitter and by careful surface treatments.

The BV_{CBO} and BV_{CES} values of this device are also identical. Data developed in this area shows an extremely tight distribution of 100 to 120 volts at 100 microamperes. The breakdown voltage requirement was initially specified at 20 milliamperes, however, because of improvements resulting from the use of the planar process, breakdown voltages can now be specified at 100 microamperes. The tight distribution combined with sharp, low current level breakdowns and identical BV_{CBO} and BV_{CEO} values

indicates a well controlled planar processing technique.

Approximately 50 percent of the emitter base junctions tested showed excellent breakdown voltages at currents below 100 microamperes. In addition, all units exceeded 8 volts at 25 milliamperes and 200°C. Most of the lower values were resistive rather than non-linear types, such as channels. The cause was therefore a high resistance ($\sim$1000 ohms) path between the emitter and base which was generally caused by photoresist failures. The three inches of emitter periphery separated by a mere 0.003 inch space between metal fingers makes this occurrence very difficult to control.

The next series of inspections made were high current dc tests. In these tests, the transistor was operated as a three-terminal device rather than as two independent diodes. The first and most important test of this series was the current gain test. Results of this test indicated that the current gain was almost independent of collector current in the 1 to 20 ampere range. The average variation of the normalized current gain was ± 4 percent in this range. The scatter diagram for a 5-ampere current gain versus values at 1 and 20 amperes reveals tight distributions, although a slight shift downward is apparent (see Figure 3). This would indicate that there is a slight peak in current gain at 5 amperes as compared to 1 and 20 amperes.

A distribution of saturation voltages at 20 amperes with an h_{FE} of 10 shows a fairly tight grouping (see Figure 22). The observation

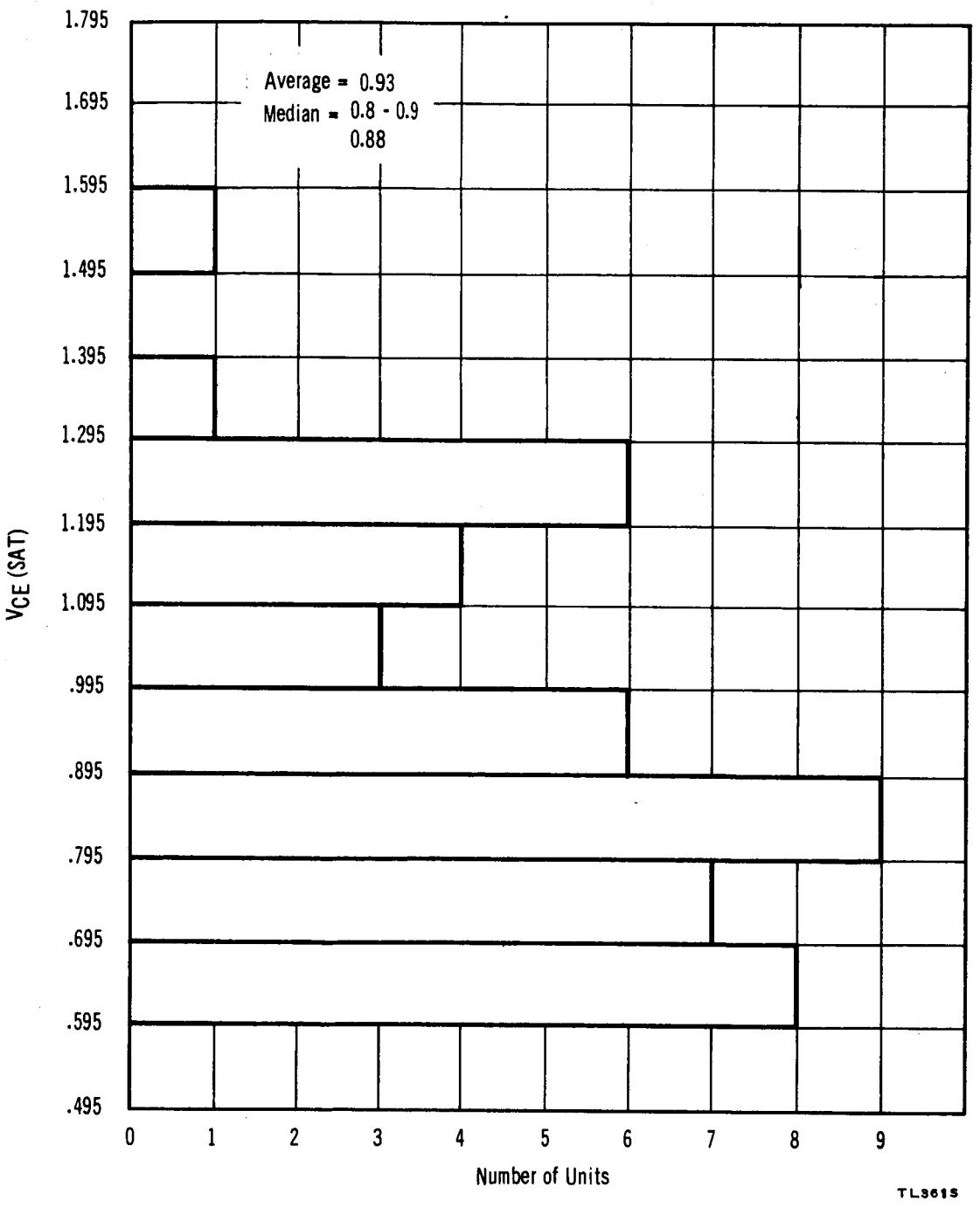


FIGURE 22 HISTOGRAM OF V_{CE} (SAT) SATURATION VOLTAGE, AT 20 AMPERES, OF FINAL UNITS

that there is an increase in this value from uncapped to capped units indicates that some of the scatter results are due to variable package resistance. All of the units shipped were below 1.5 volts. The average voltage was approximately 0.85 volt. This is a very good value for triple-diffused, silicon power transistors. The V_{BE} saturation voltages were quite uniform. Virtually every unit was between 1.3 and 1.5 volts.

The most important measurement made on this transistor was switching time. To meet contract requirements the total on-time and total off-time of the device had to be less than 250 nanoseconds. The turn-on times were extremely uniform, ranging in value from 130 nanoseconds to 180 nanoseconds and they were probably inductively limited. However, the turn-off times were more difficult to achieve. Section III-10 shows that this value is dependent on several independent parameters; common emitter gain, base width, collector thickness, and lifetime. The values are therefore spread much wider than those for turn-on time. The important factor, however, is that every unit delivered had an on-time and off-time of less than 300 nanoseconds and all but four units were below 260 nanoseconds (see Figure 23). The median value was 205 nanoseconds while the median value of the storage time part of the trace was 160 nanoseconds. The experiments made on lifetime reducing techniques along with the knowledge obtained on the critical parameters leads to the belief that future devices can be made to turn off considerably faster.

The output capacitance measured at 10 volts was made mainly to record the parameter. It was in agreement with both empirical and calculated

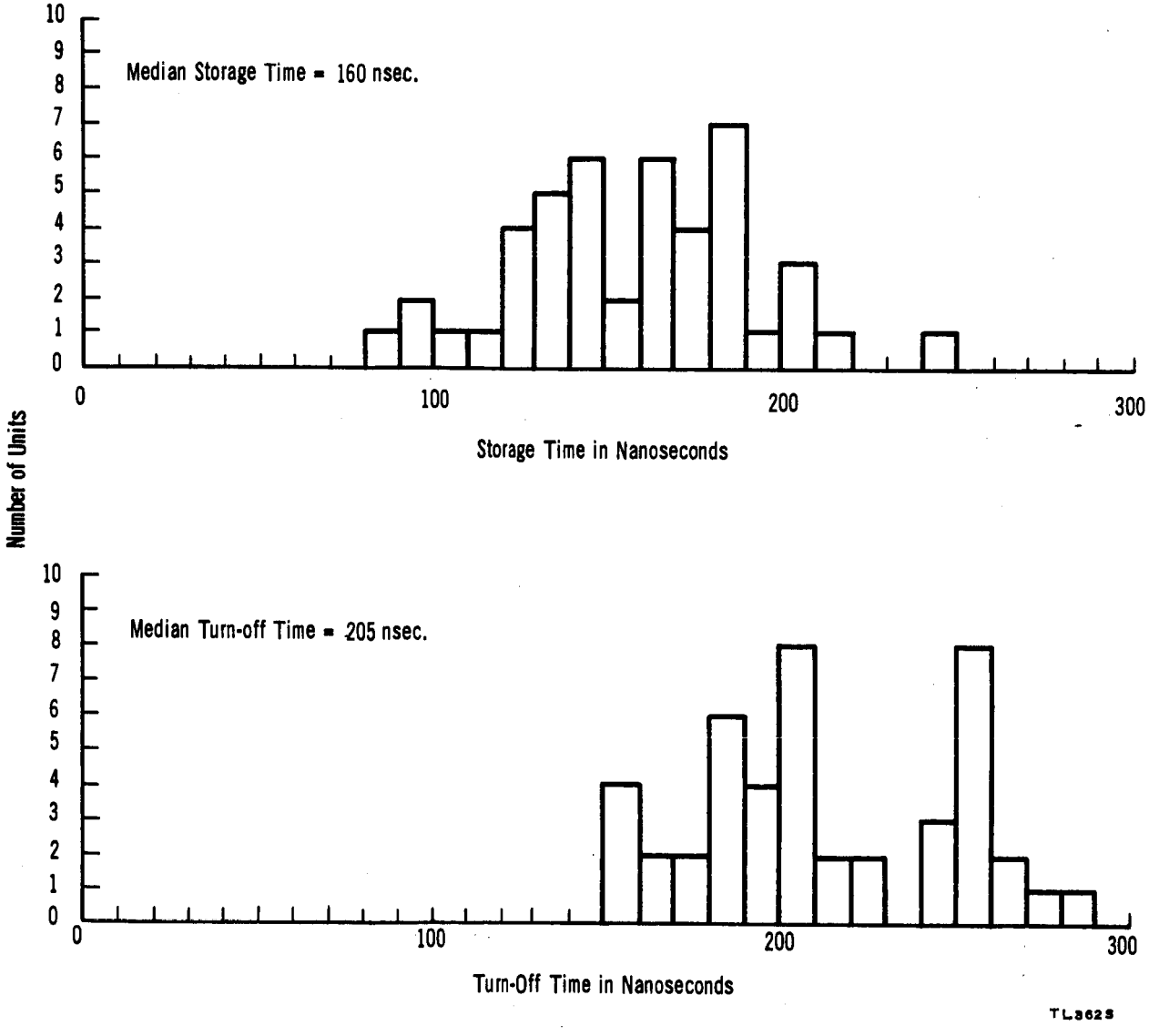


FIGURE 23 HISTOGRAM SHOWING STORAGE TIME AND TURN-OFF TIME OF FINAL UNITS

values for the resistivity and area of this device.

The thermal resistance of the devices packaged in an isolated collector 11/16" DES case is shown in Figure 1. The relative tightness of the distribution indicates that both alloying interfaces and the beryllium oxide pellets were under control. The values obtained show excellent agreement with the calculated value which,in turn,show that the mounting operations were optimized. The average value of thermal resistance was $1.17°C/_{W}$.

VII. CONCLUSIONS AND RECOMMENDATIONS

The contract requirements of this program have been successfully met by the development of a large area planar silicon transistor. The major difficulties common to the fabrication of large area planar diffused junctions, with breakdown voltages in excess of 100 volts and reverse currents of less than 50 nanoamperes were solved by the development of new processing techniques. Random defects were eliminated by exercising stringent control over diffusion and masking techniques and by improved metal contact processing. This elimination resulted in devices with high yields. Devices with base areas of 19,000 $mils^2$ were made at diffusion yields of 50 percent.

An isolated collector package was designed, utilizing beryllium oxide as the insulating material. This package is easy to fabricate, rugged and capable of dissipating 100 watts at a case temperature of 100°C.

The requirement, that the device switch 20 amperes in less than 0.25 microseconds, was achieved by utilizing a device design with a low ratio of base area-to-emitter length, low current gain and a narrow collector region.

Studies made on optimizing transistor geometries by the overlay technique have revealed that this is feasible. An increased effort in this area should result in devices which combine fast transient characteristics with high power handling capacities.

A program designed to study the reliability of large area planar devices, as compared to mesa type structures, is recommended. It is felt that these devices are inherently more reliable. However, the number of devices available, during the contract period, was not sufficient to make detailed environmental studies.

Further study of the effects of radiation on device characteristics is recommended. Such a study should include stability tests and initial effects on device parometers.

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